Multi-element Silicon Detectors for X-ray Spectroscopy and Diffraction

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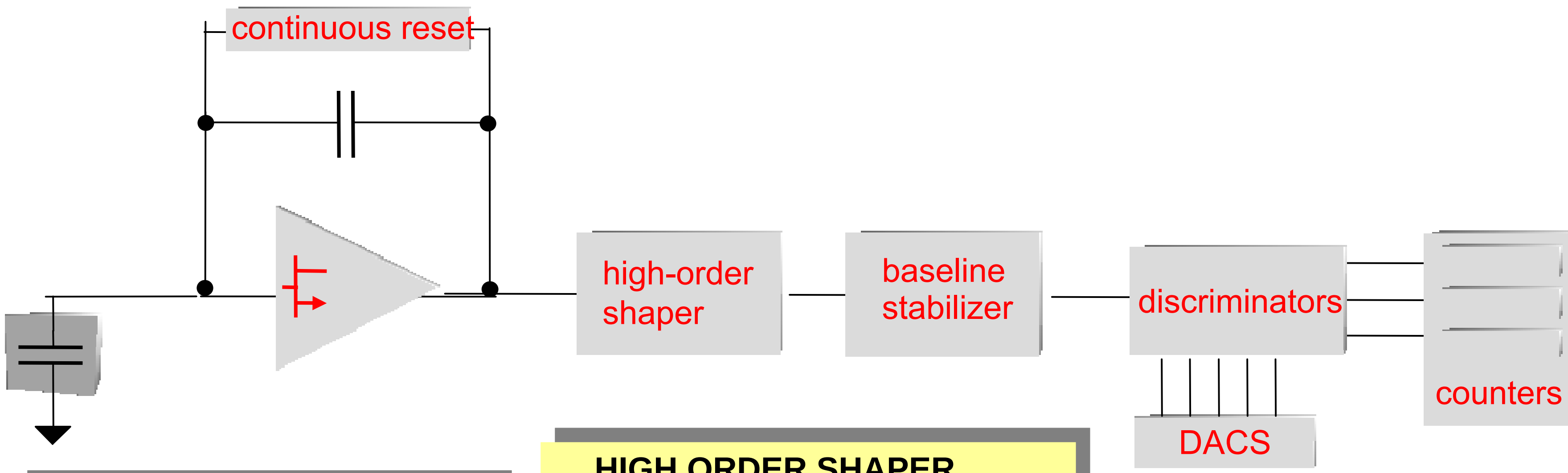
BNL Collaborators for silicon detector development

- Zheng Li , Pavel Rehak, Wei Chen, Rolf Beuttenmuller, detector elements (Inst. Div.).
- Paul O'Connor, Gianluigi De Geronimo, ASIC design (Inst. Div).
- Peter Siddons, Tony Kuczewski, computer and user interface (NSLS)
- Technical assistance:
  - John Triolo, Don Pinelli (Inst.) ,
  - Denis Poshka, Tony Lenhard, Shu Cheung, Rick Greene (NSLS)

Outline

- The HERMES ASIC
  - design
  - spectroscopic performance
- Detector elements
  - charge sharing
- Next steps for spectroscopy
- HERMES + strip detector
  - Powder diffraction
  - GISAXS
- Next steps for strip arrays

HERMES chip organization



INPUT p-MOSFET

- optimized for operating region
- NIM A480, p.713

CONTINUOUS RESET

- feedback MOSFET
- self adaptive 1pA - 100pA
- low noise < 3.5e$^-$ rms @ 1μs
- highly linear < 0.2% FS
- US patent 5,793,254
- NIM A421, p.322
- TNS 47, p.1458

HIGH ORDER SHAPER

- amplifier with passive feedback
- 5th order complex semigaussian
- 2.6x better resolution vs 2nd order
- TNS 47, p.1857

BASELINE STABILIZER (BLH)

- low-frequency feedback, BGR
- slew-rate limited follower
- DC and high-rate stabilization
- dispersion < 3mV rms
- stability <2mV rms @ rt×tp<0.1
- TNS 47, p.818

DISCRIMINATORS

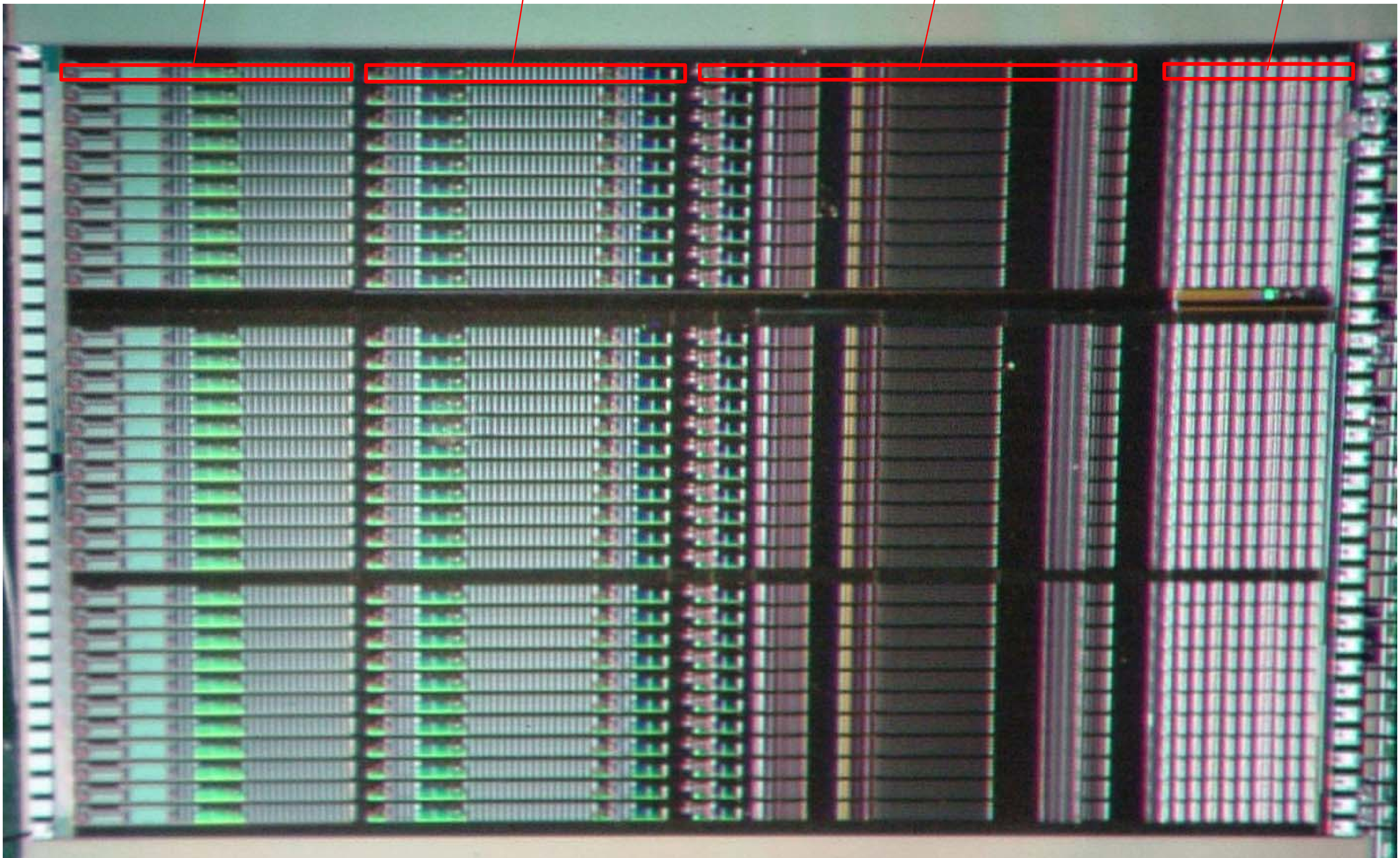
- five comparators
- 1 threshold + 2 windows
- four 6-bit DACs (1.6mV step)
- dispersion (adj) < 2.5e$^-$ rms

COUNTERS

- three (one per discriminator)
- 24-bit each

≈ 3 mW ≈ 5 mW

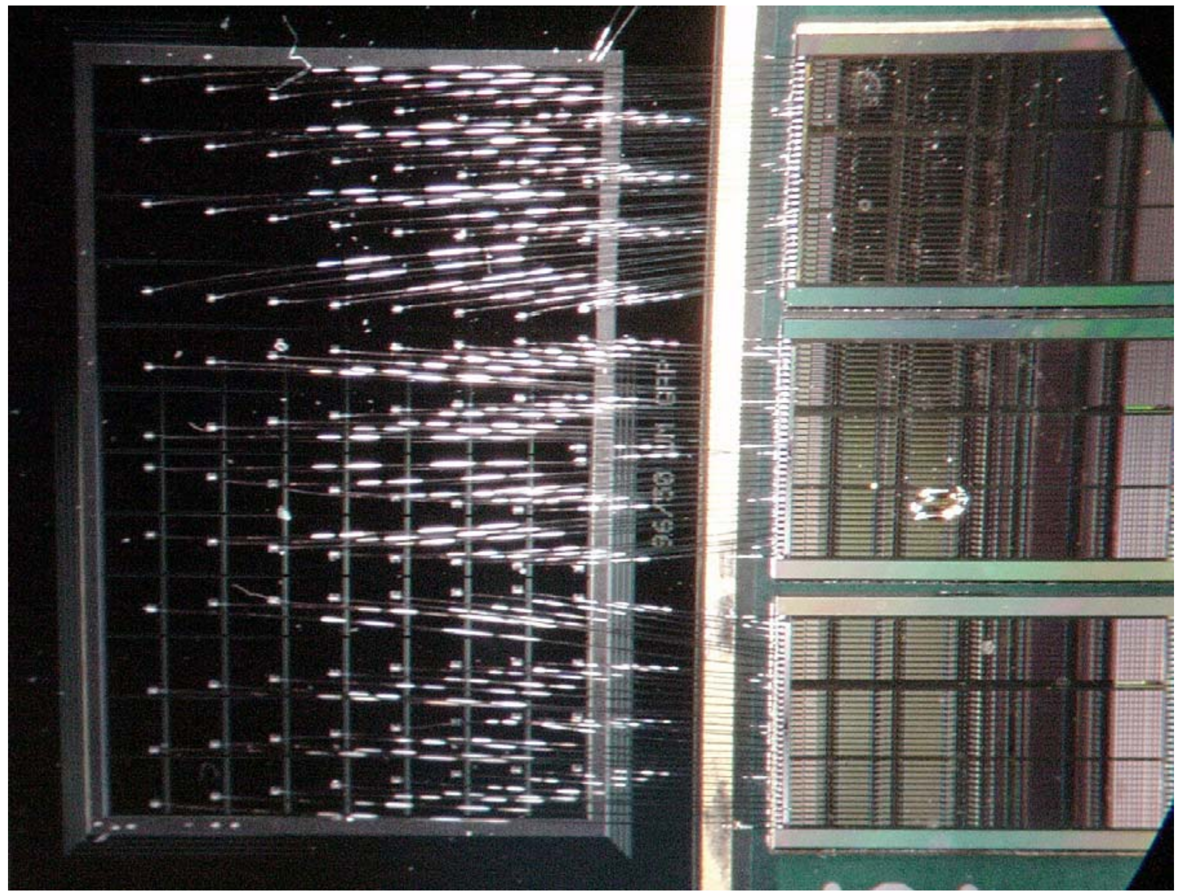
'HERMES' ASIC photo



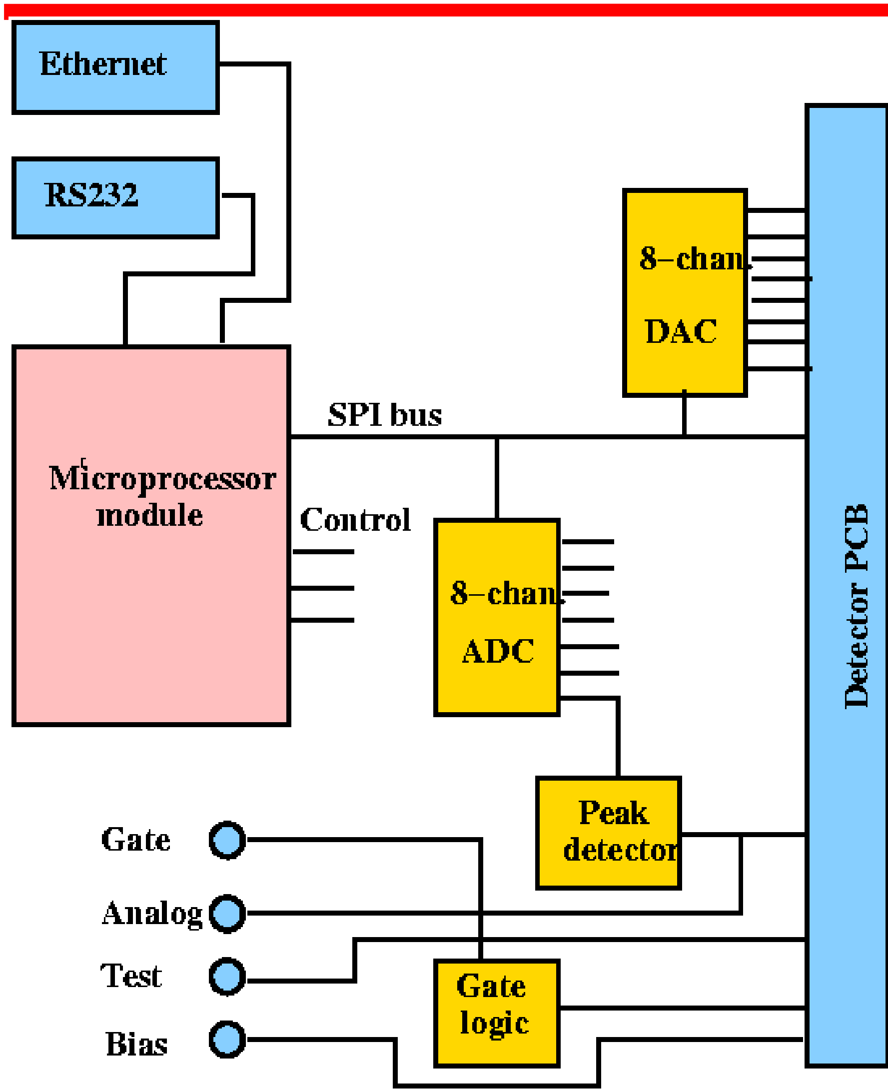
32 channels, 3.6 × 6.3 mm²

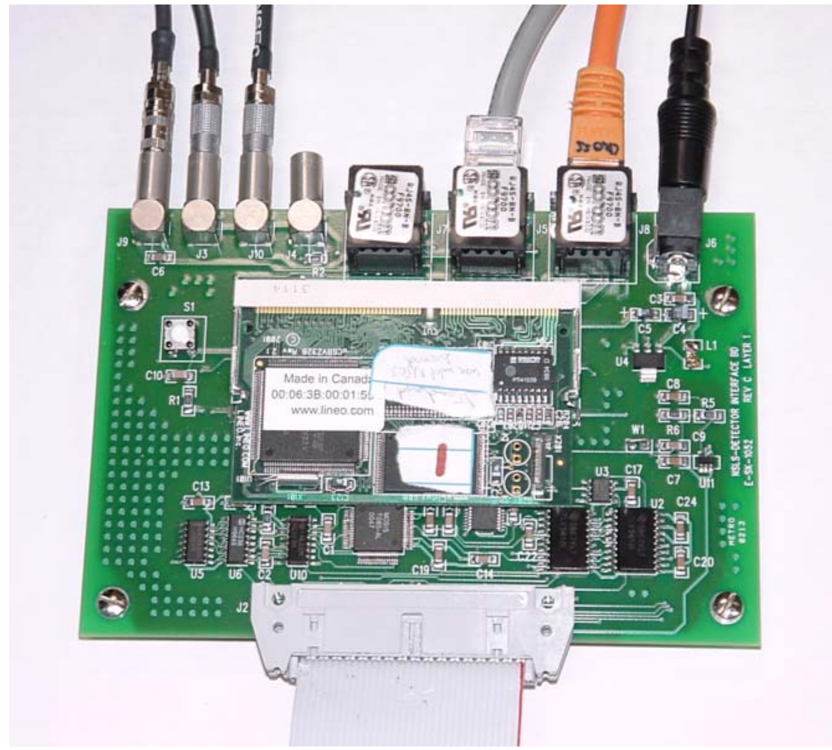
One quadrant with ASICS

- 96 pads wire-bonded to 3 ASICS.
- The long bonds are rather fragile, but this approach provided least parasitic capacitance.
- Each ASIC provides 32 channels of low-noise analog/digital processing.
- ASIC appears to have 100% yield (no bad channels to date).



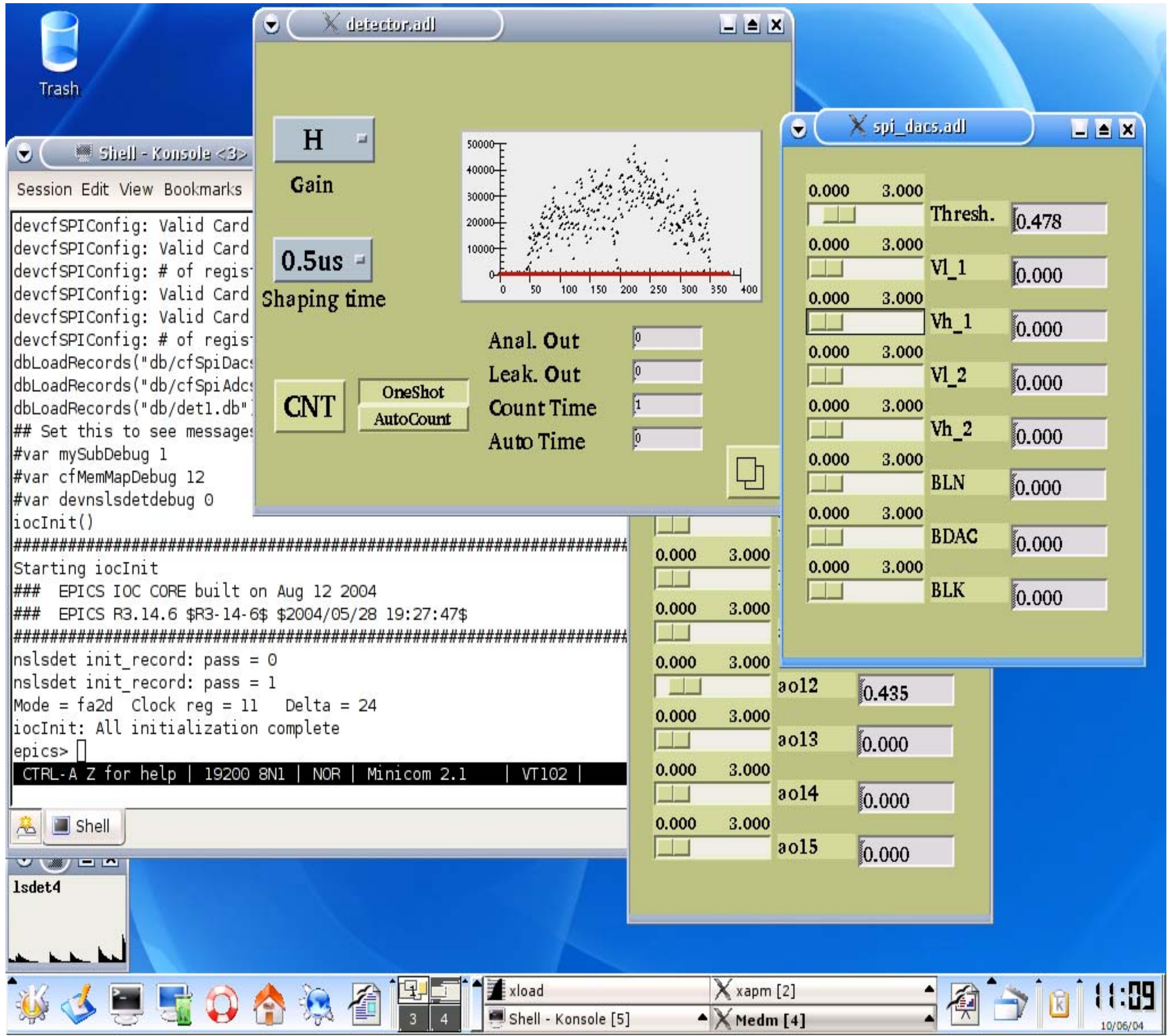
Controls


Ethernet
RS232
8-chan.
DAC
SPI bus
Microprocessor module
Control
8-chan.
ADC
Detector PCB
Peak detector
Gate
Analog
Test
Bias
Gate logic



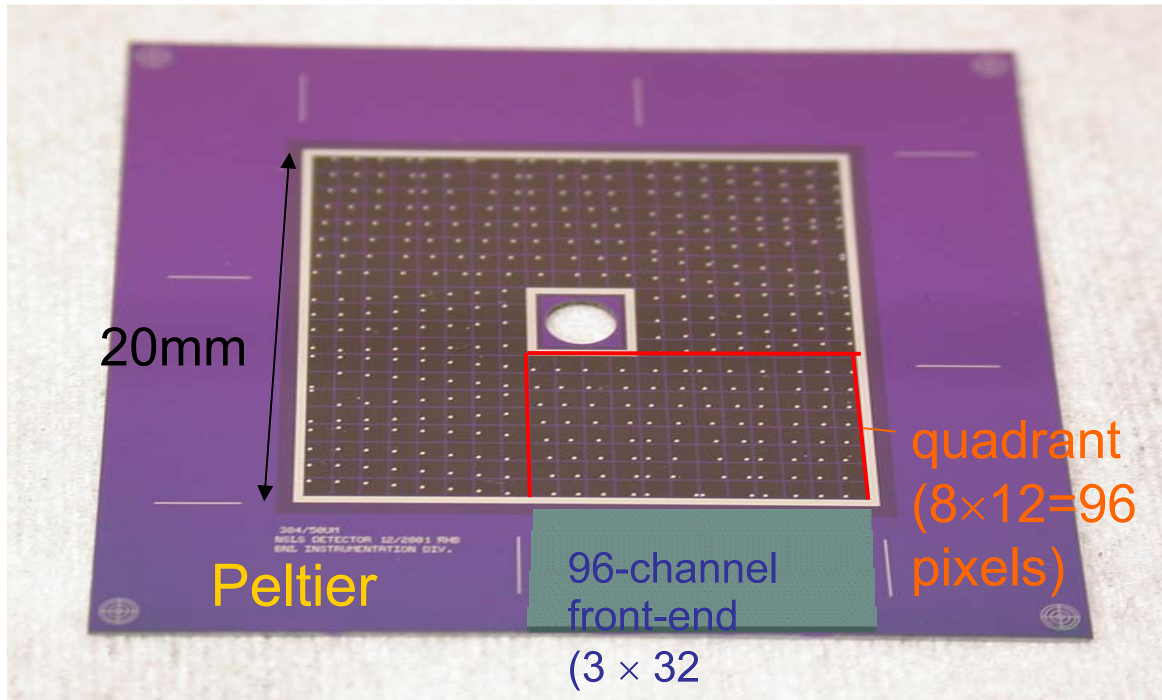
MEDM user interface

- SOFTWARE IS IMPORTANT!!!
- Standard EPICS facilities allow quick GUI development, much easier than conventional GUI toolkits.
- Device looks very similar to the standard EPICS scaler device, but with many more channels and additional detector control functionality.
- Thresholds set via on-board DACs accessed as 'ao' records.

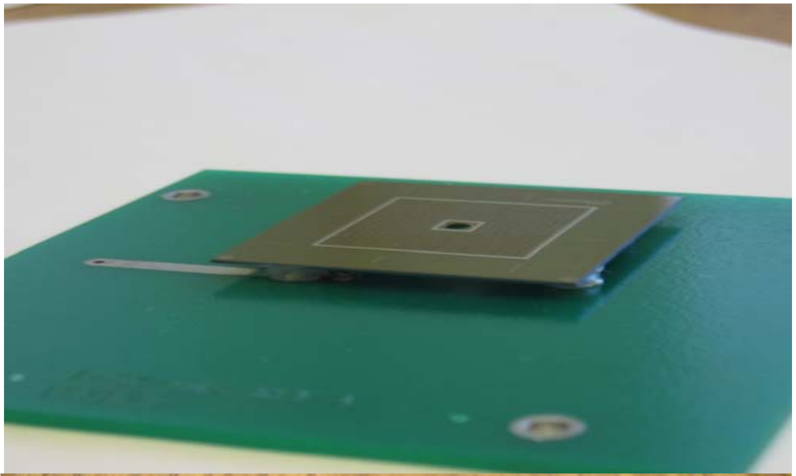


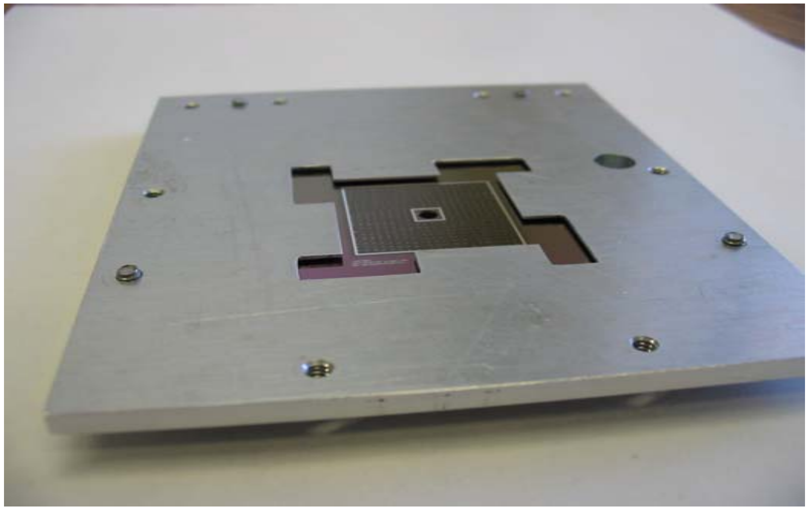
High-rate multi-element detector for fluorescence measurements

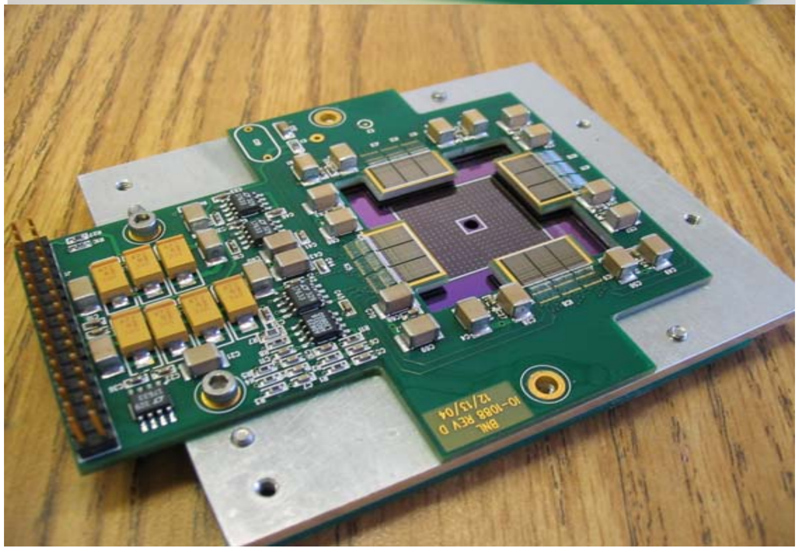
- 398-element silicon pad array for absorption spectroscopy and/or x-ray microprobes.
- Central hole for incident pump beam to allow close approach to sample.
- Uses 12 ASICS.
- Peltier cooled to -35 deg. C.

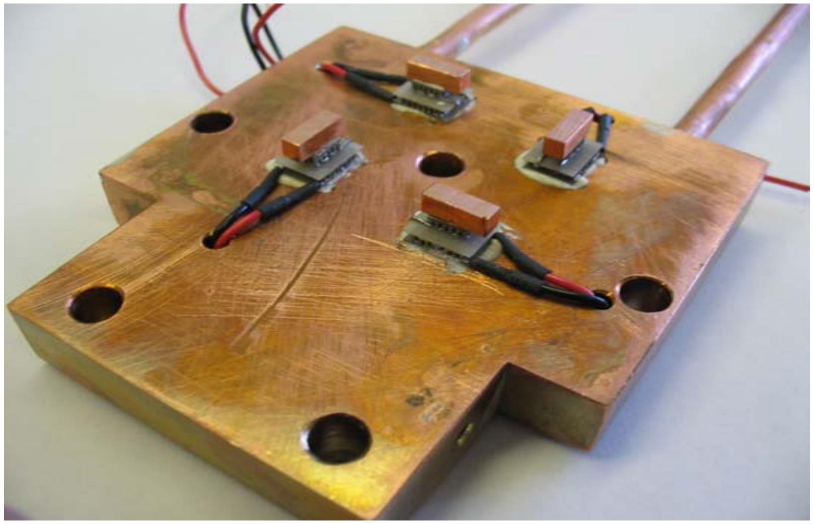


Assembly

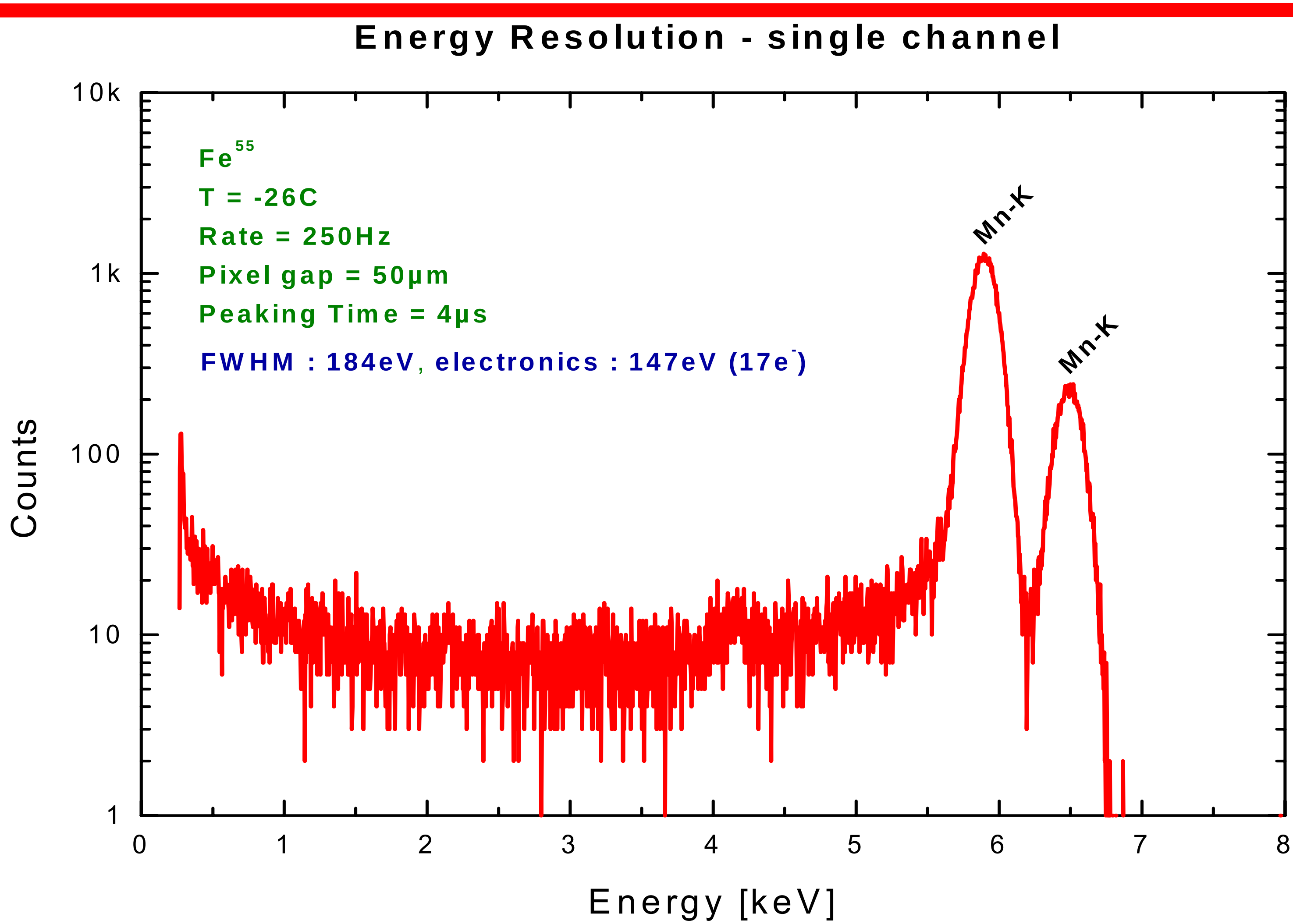








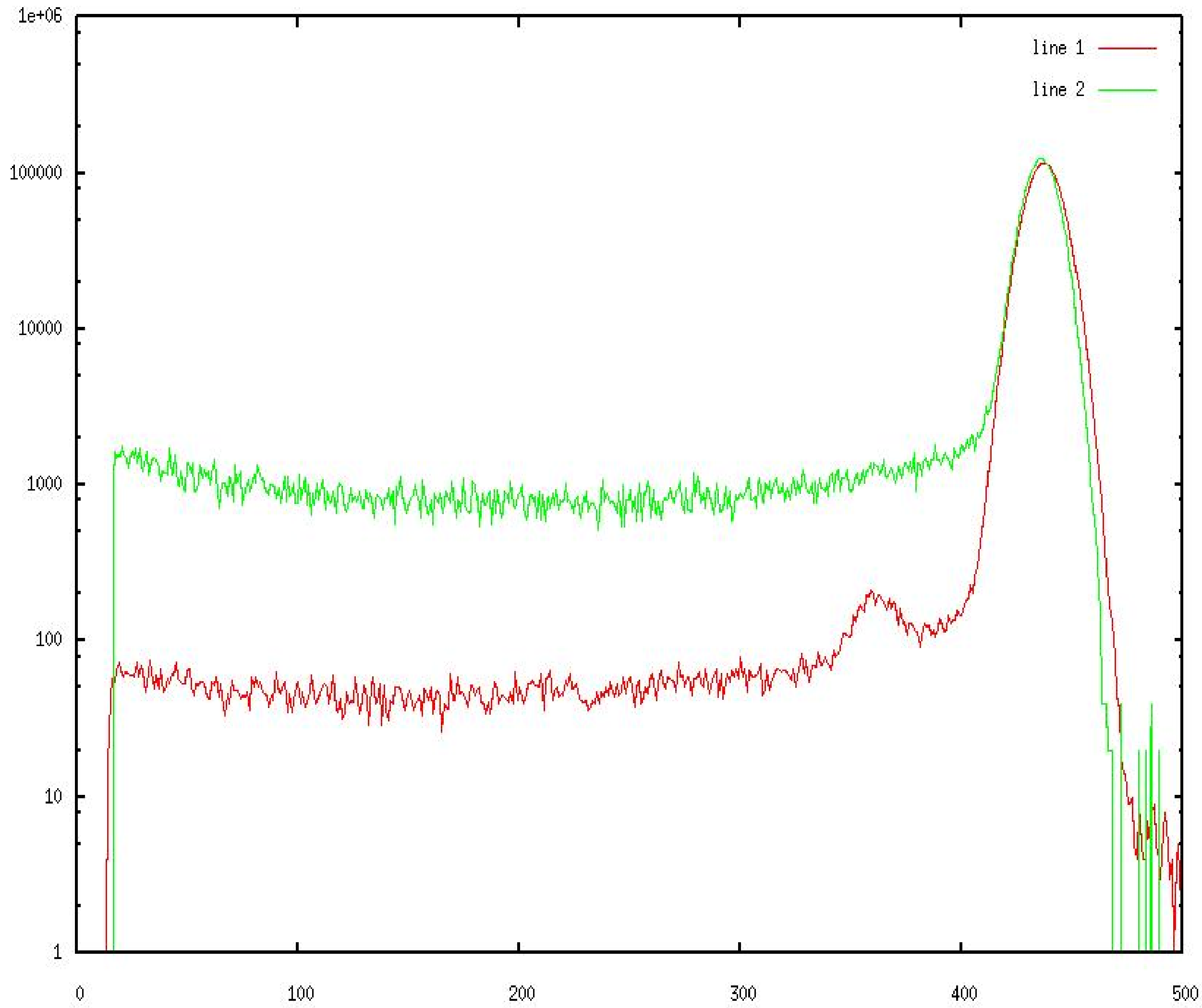
^{55}Fe spectrum



50µm-gap, $C_p \approx$ 700fF, $C_{i\text{-bond}} \approx$ 50-200fF, $C_{i\text{-pad}} \approx$ 220fF

Charge-sharing

- Pinhole collimator measurements:
  - Green curve near edge of pixel
  - Red curve at center of pixel
- Primarily a geometrical problem
  - Absorption mask to cover gaps
  - 'Trenching' to physically separate pixels, at least on entrance side.



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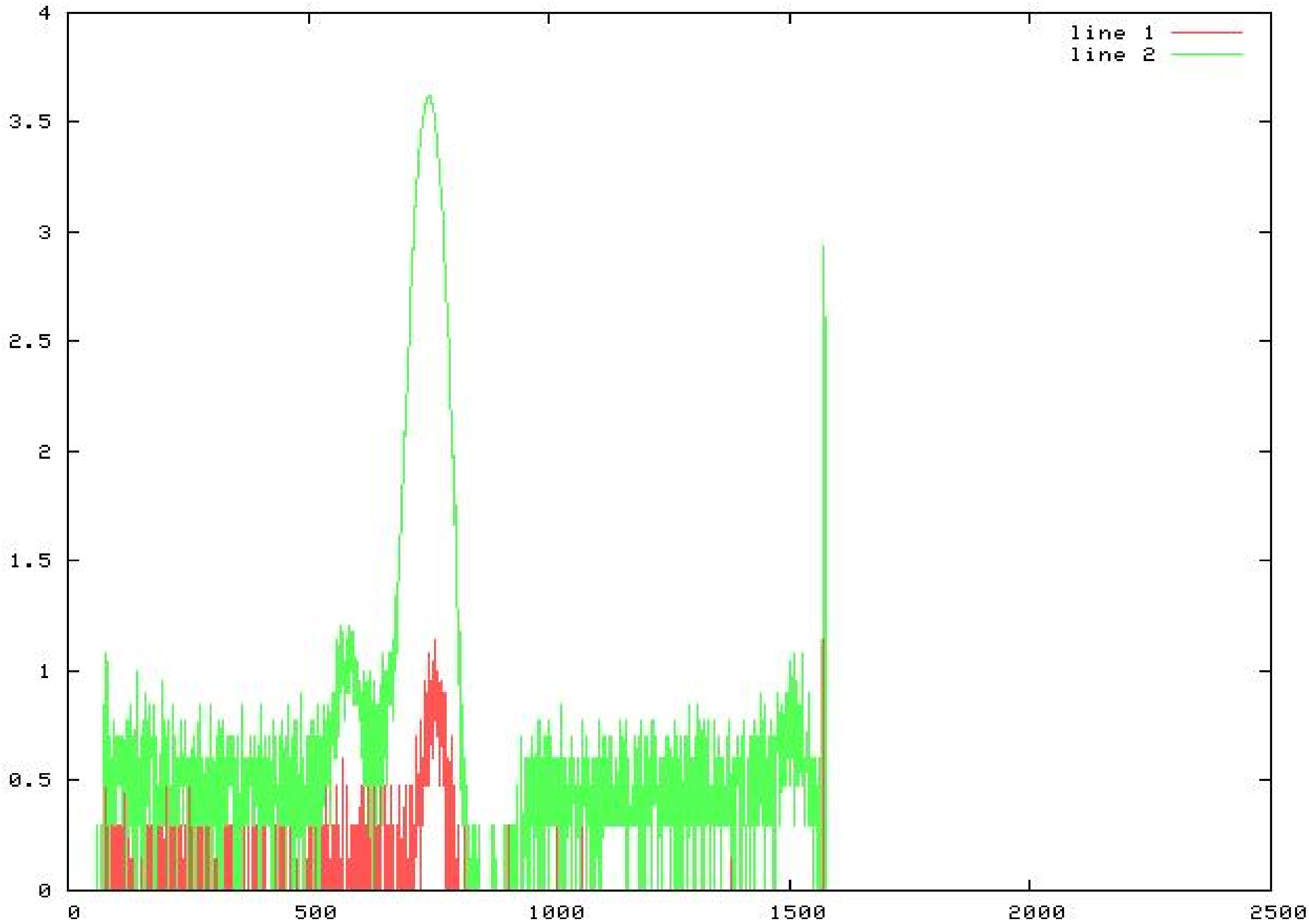
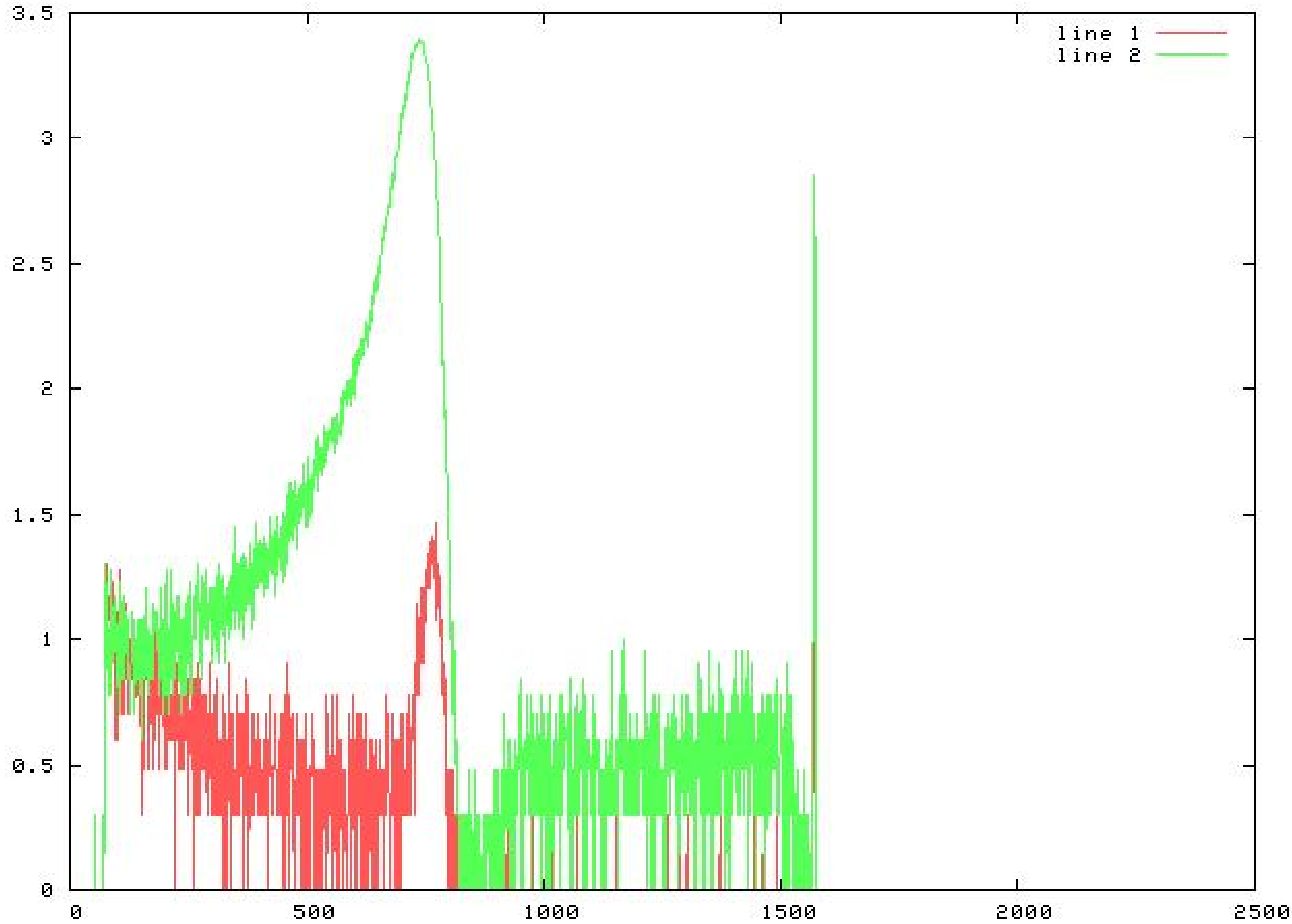
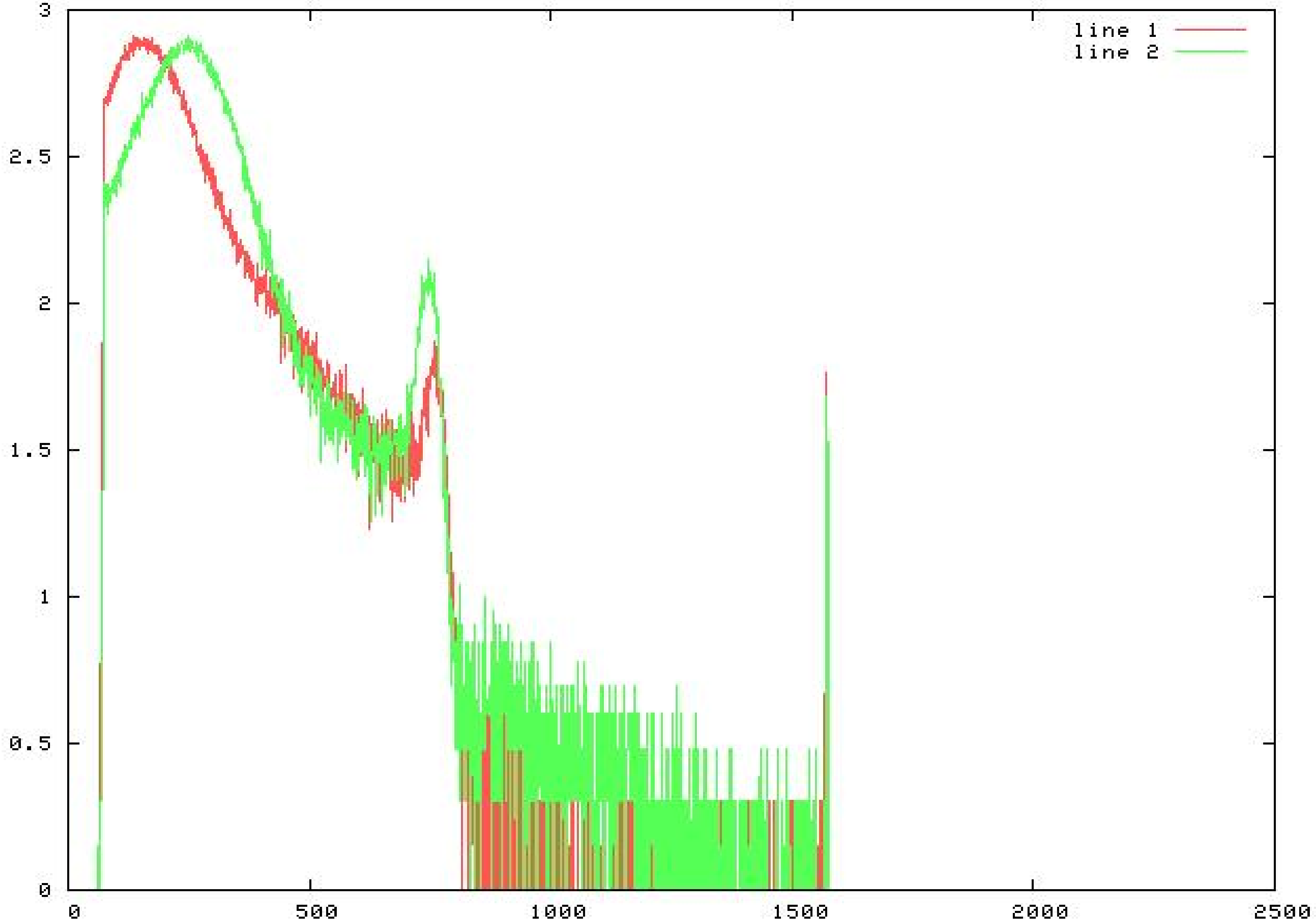
Charge sharing



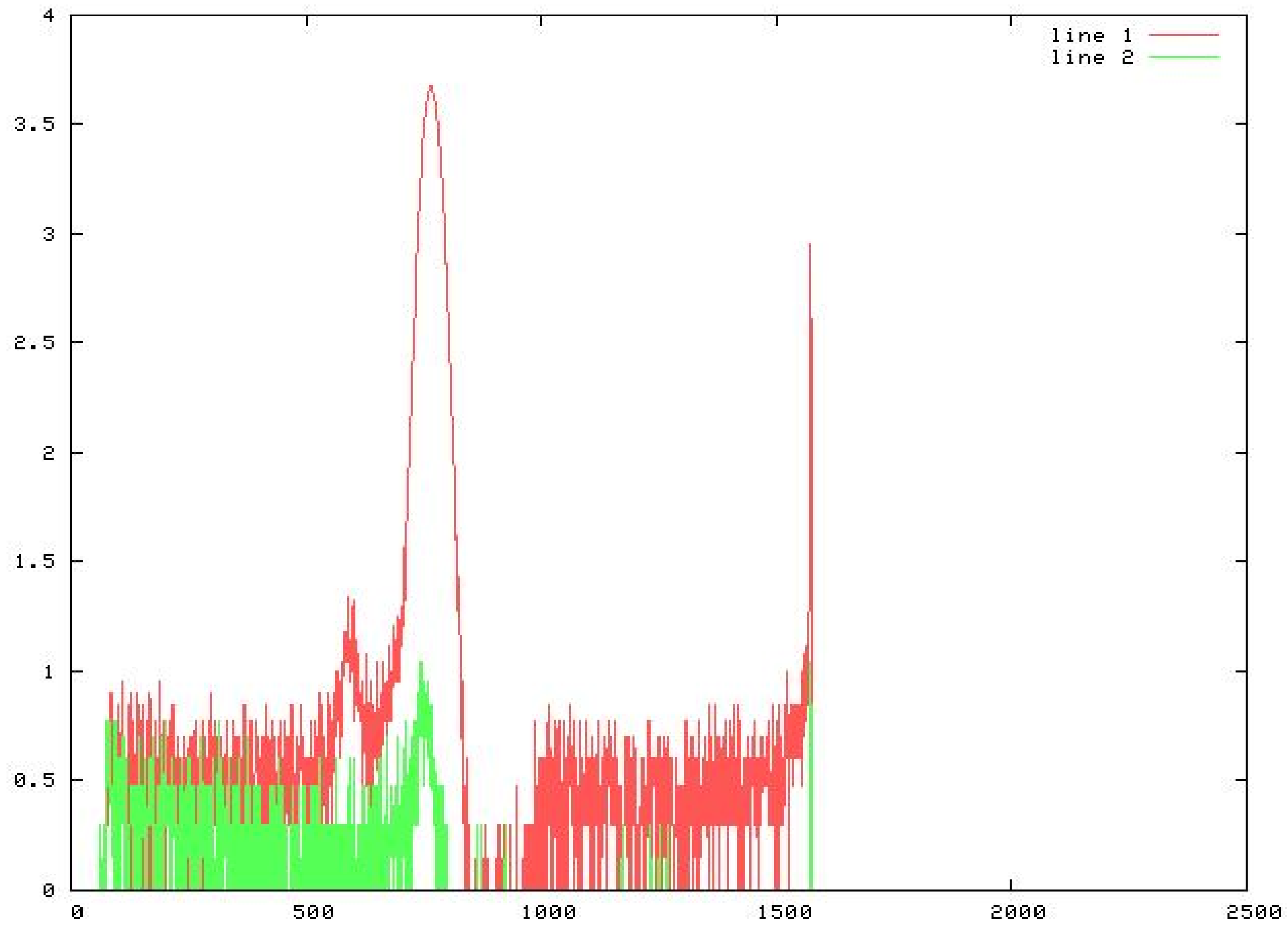
Charge sharing



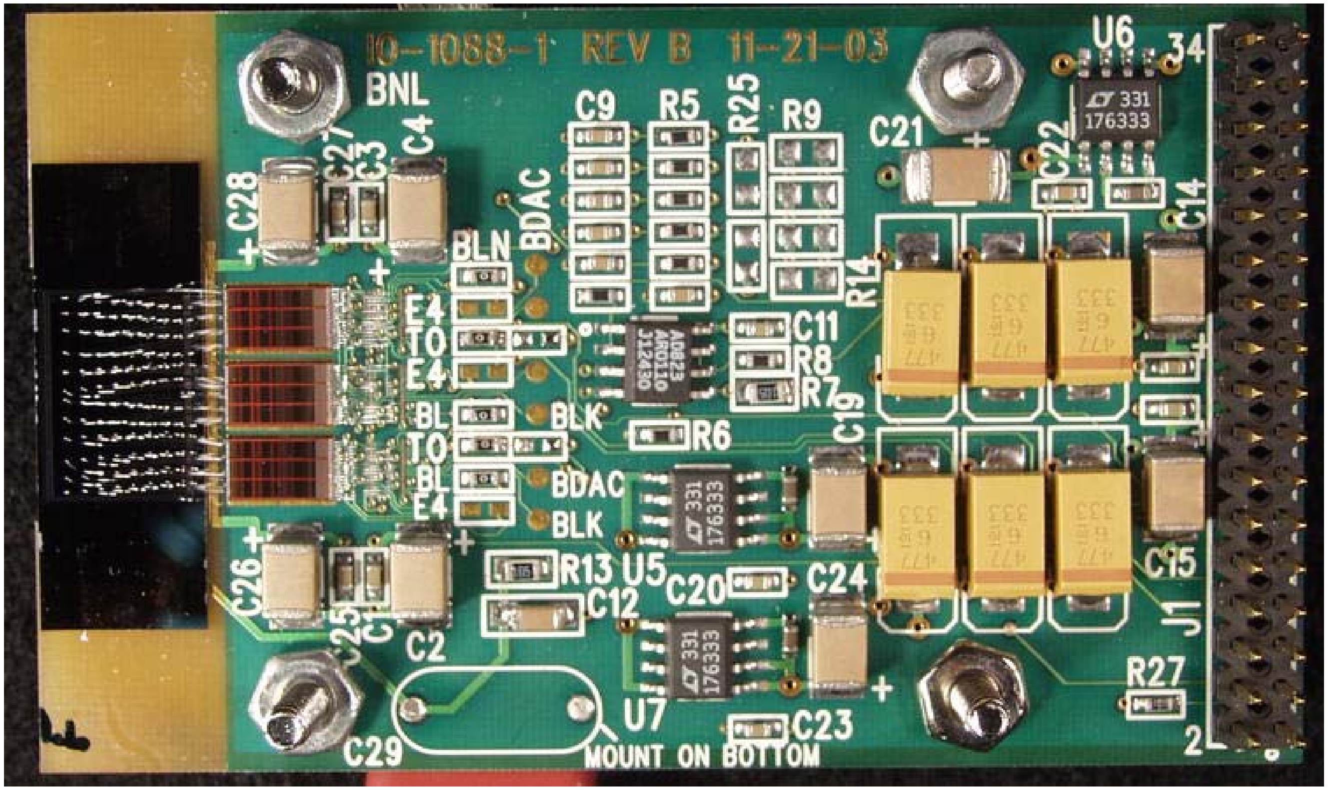
Charge sharing



Charge sharing

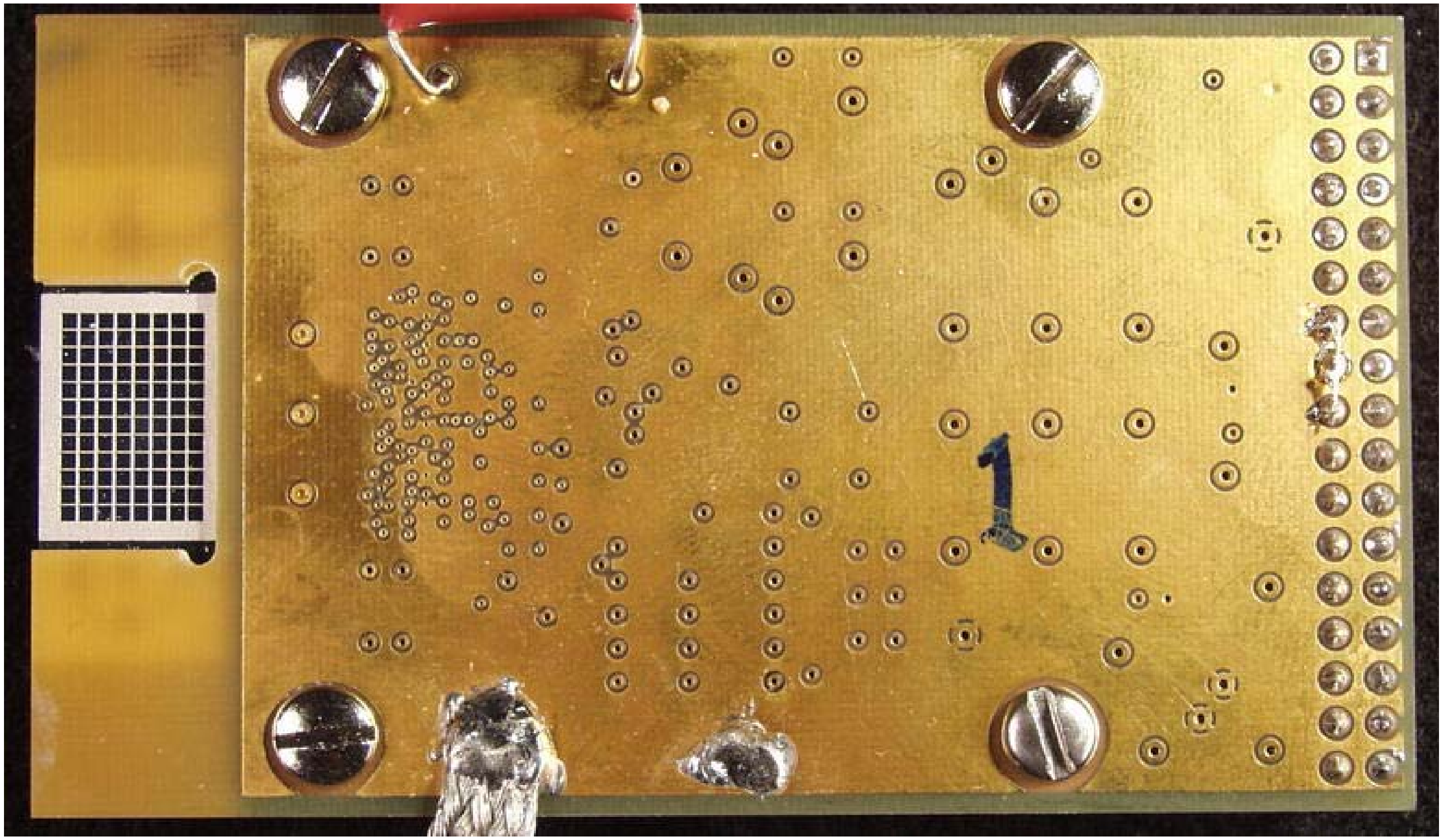


Pad side 96-channel detector



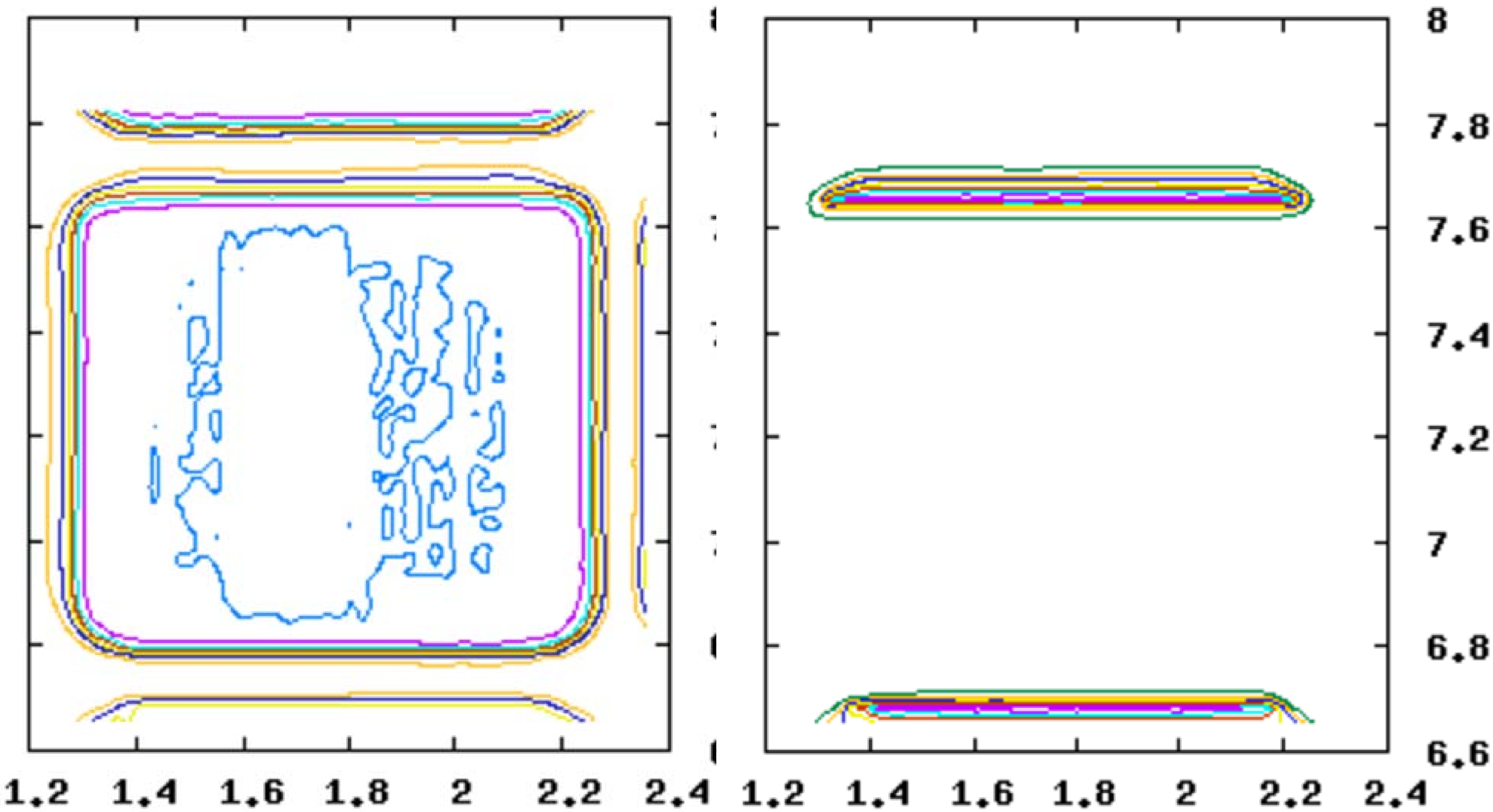
- 3 chips wire-bonded to 96 pads, each 1mm x 1mm.

Absorbing mask



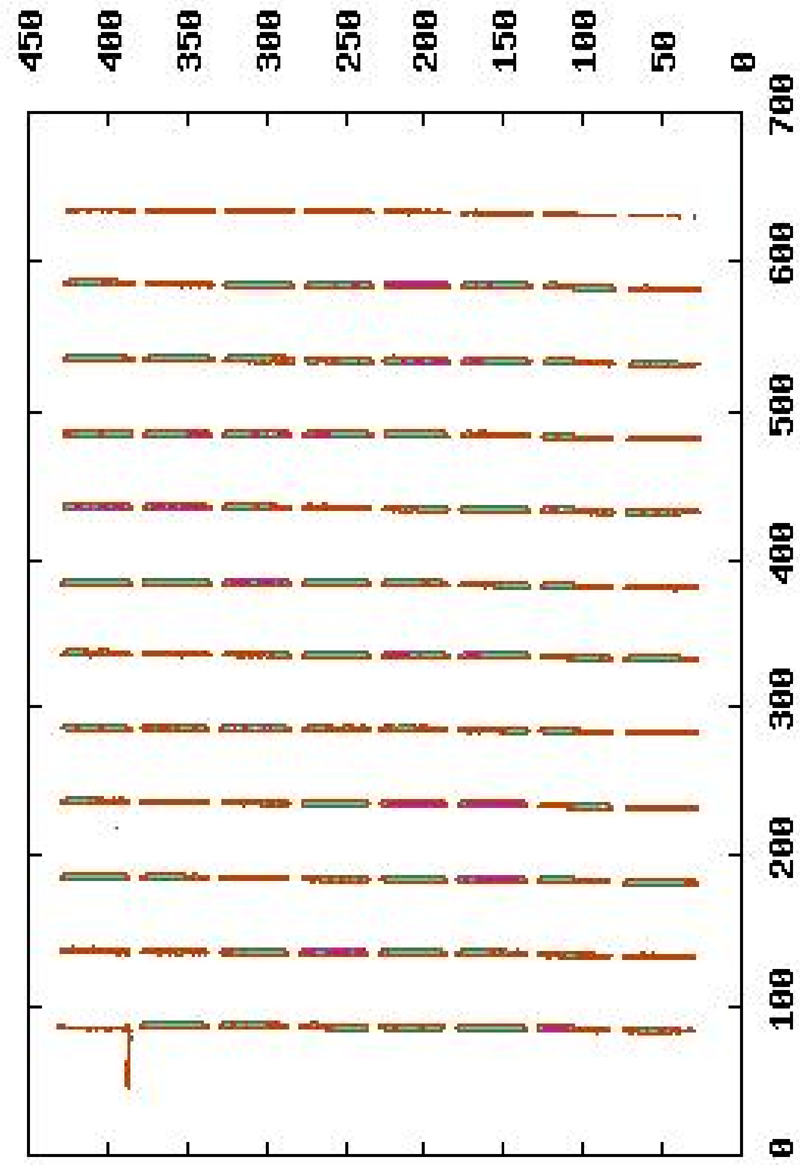
- 0.1mm thick Mo, with 0.1mm wide absorbing strips between pixels.
- Chemical machining (Towne Technologies, NJ)
- Aligned under microscope and glued in place

Sharing map



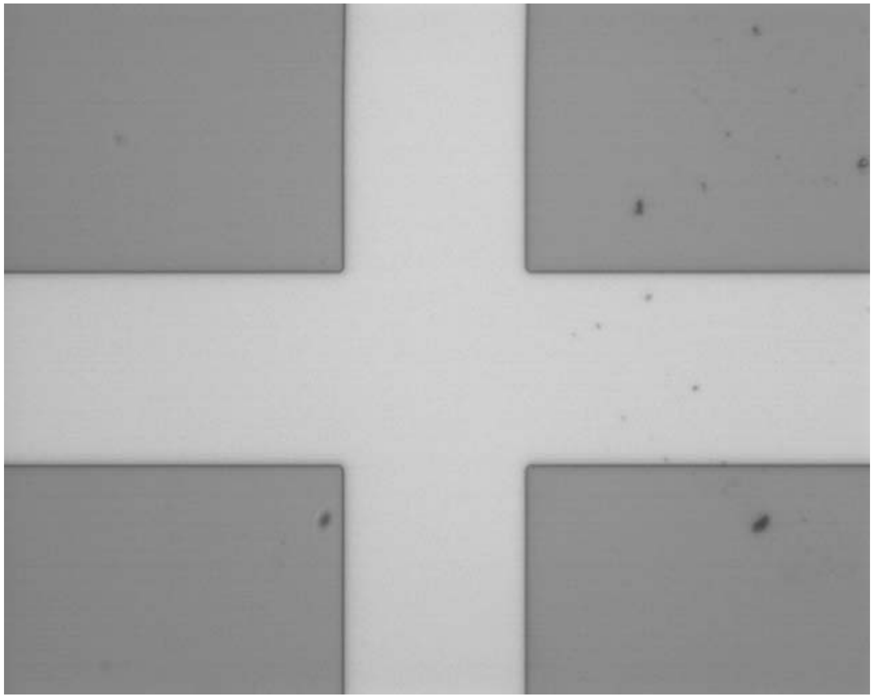
Whole detector scan

- Mask is 'perfectly' misaligned!

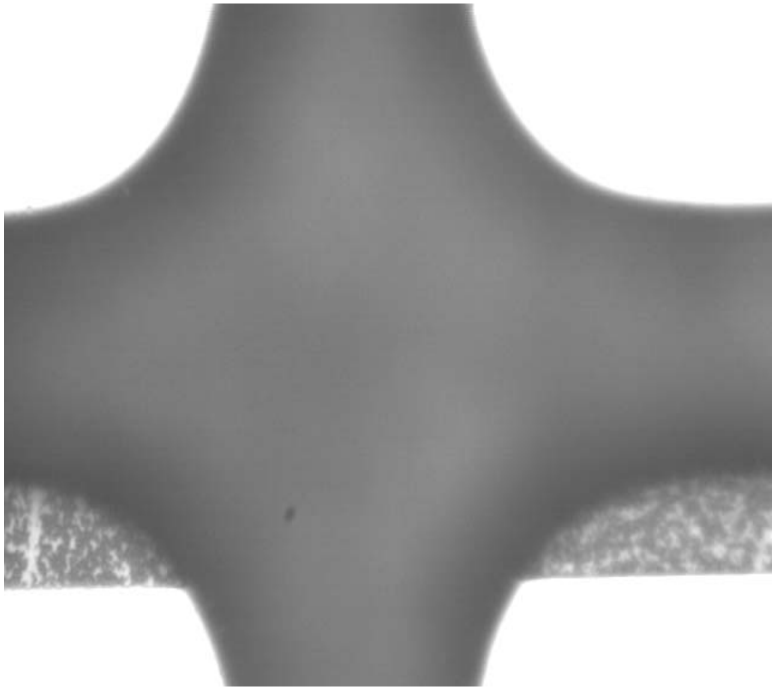


Micrographs

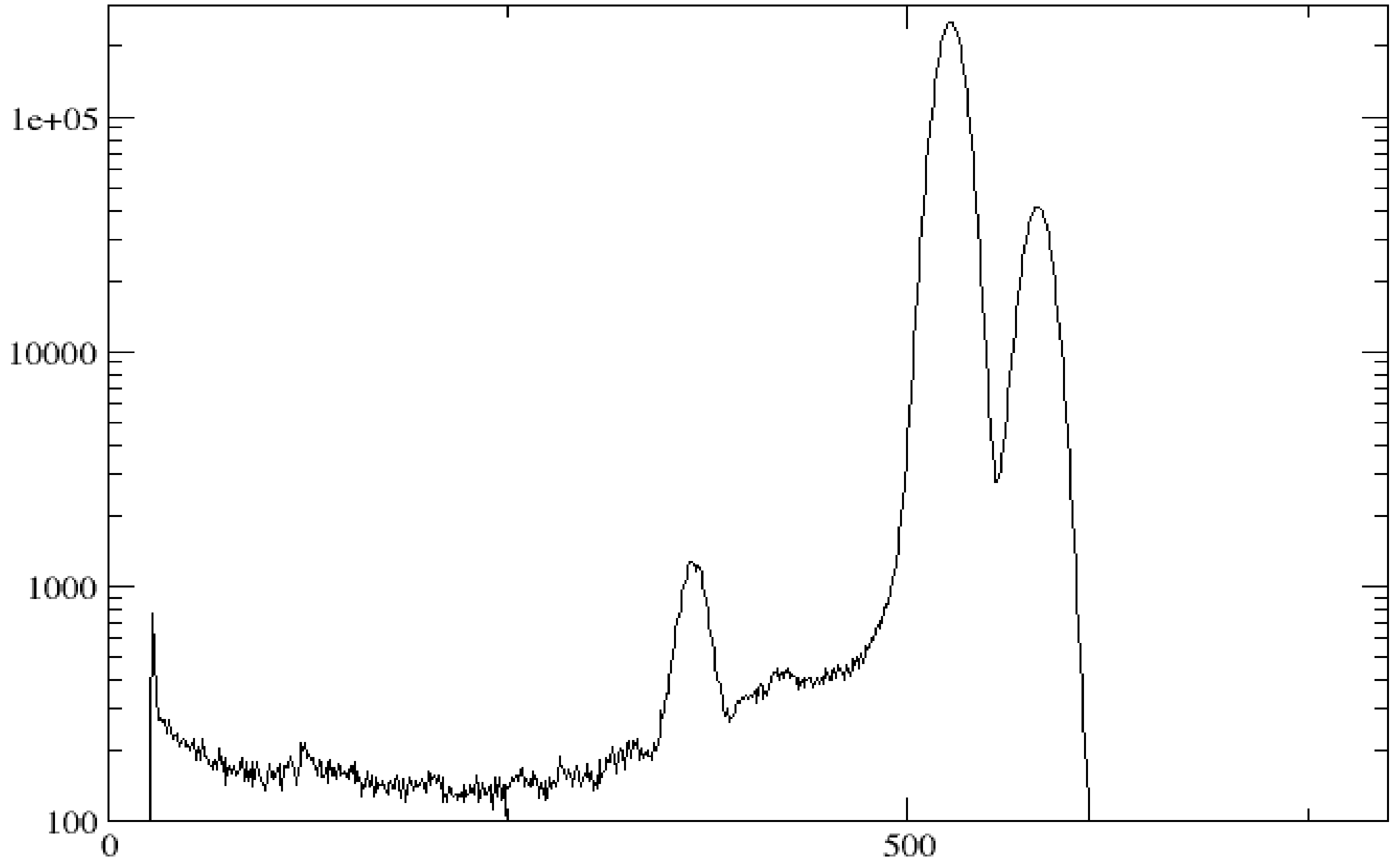
- Diode implant side showing inter-pixel gaps



- Misaligned absorber mask



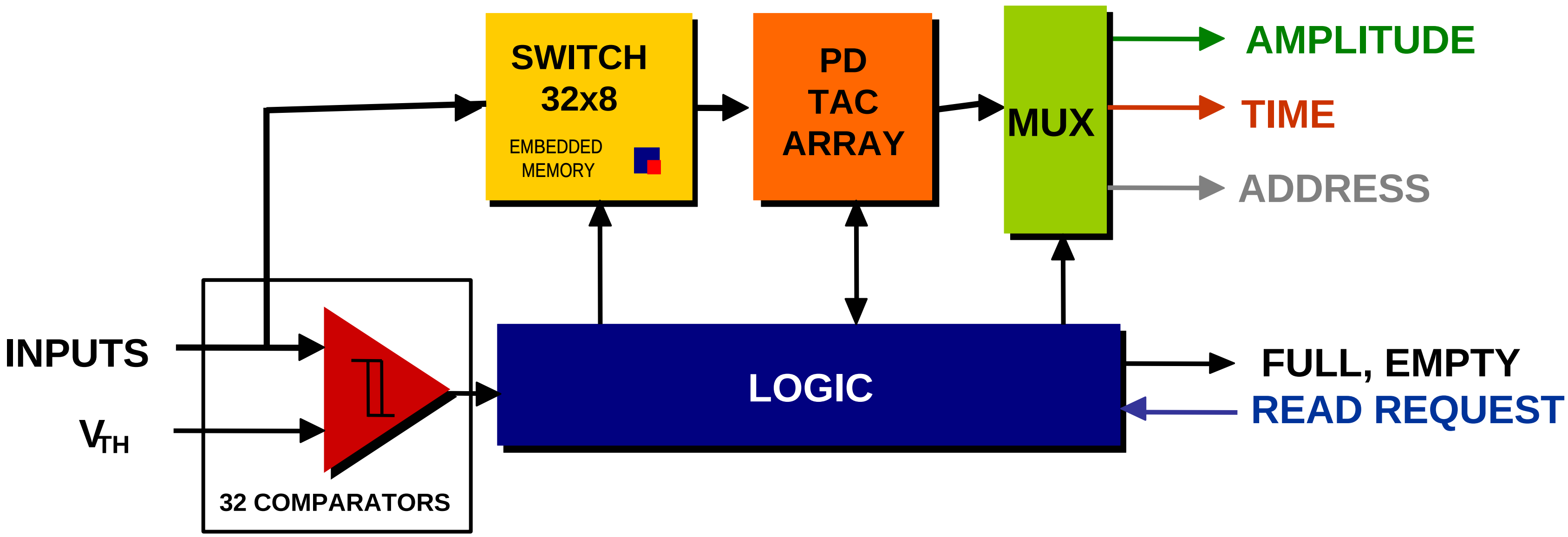
Flood ^{55}Fe spectrum with properly aligned mask



Next steps for spectroscopy

- Work towards a system providing full spectrum per channel, instead of hardware windows
  - Same low-noise analog front-end
  - Integrate BNL Peak-detect / derandomizer module, modified for time-over-threshold mode.
  - Fast ADC + FPGA + CPU to process data
- Real-time processing of data for microprobe applications (collaboration with Chris Ryan, CSIRO Australia)
- Try to replace pad detectors with drift detectors.

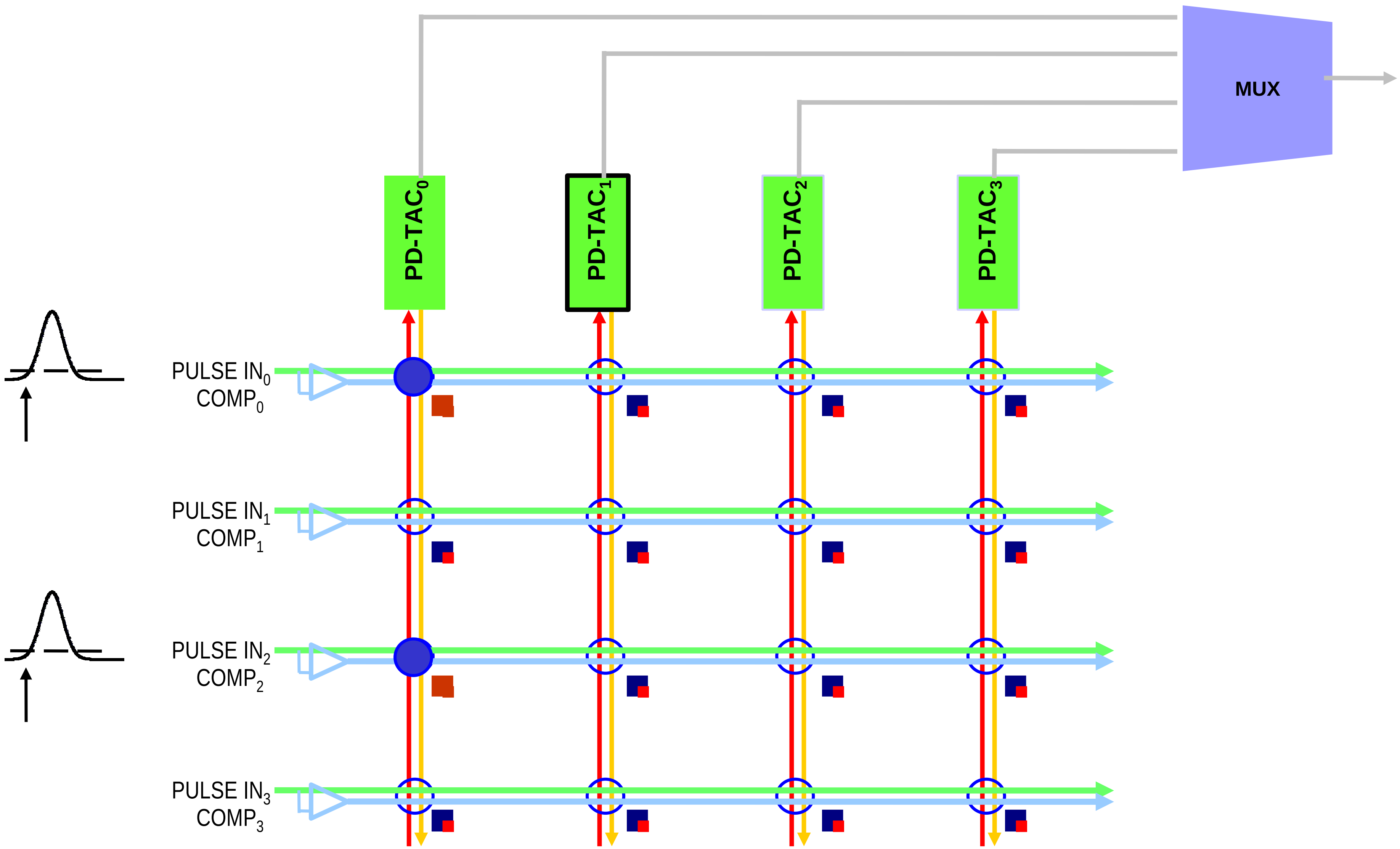
The Peak Detector Derandomizer ASIC Architecture
(A. Dragone, G. De Geronimo, P. O'Connor)



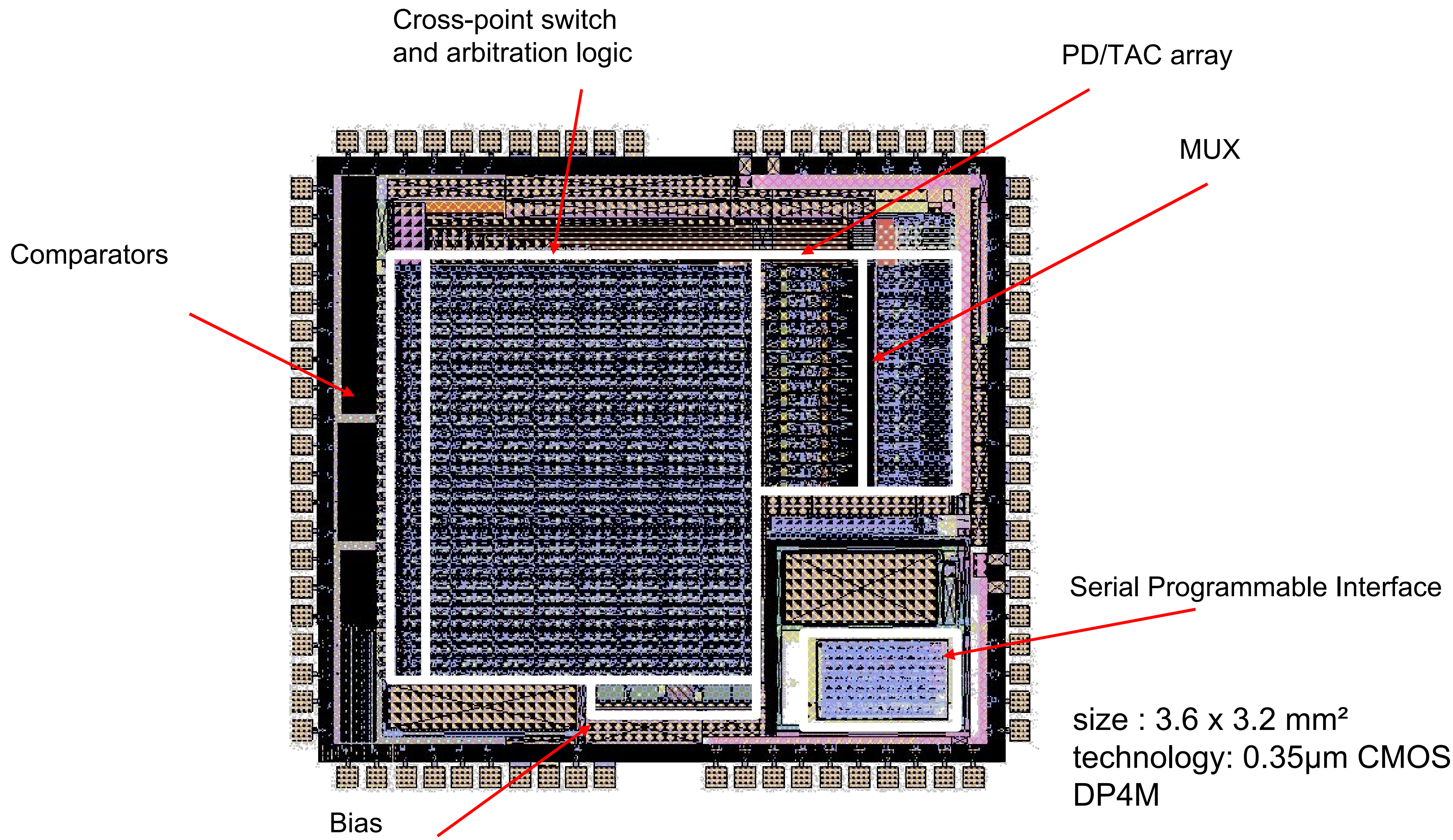
- New architecture for efficient readout of multichannel detectors
  - *Self-triggered and self-sparsifying*
  - *Simultaneous amplitude, time, and address measurement for 32 input channels*
  - *Set of 8 peak detectors act as derandomizing analog memory*
  - *Rate capability improvement over present architectures*
- Based on new 2-phase peak detector combined with Quad-mode TAC
  - *High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)*
  - *Accepts pulses down to 30 ns peaking time, 1.6 MHz rate per channel*
  - *Low power (2 mW per channel)*

P. O'Connor, G. De Geronimo, A. Kandasamy, *Amplitude and time measurement ASIC with analog derandomization: first results*, IEEE Trans. Nucl. Sci. 50(4), pp. 892-897 (Aug. 2003).

The Switch matrix + Simultaneous Events Catcher (SEC)



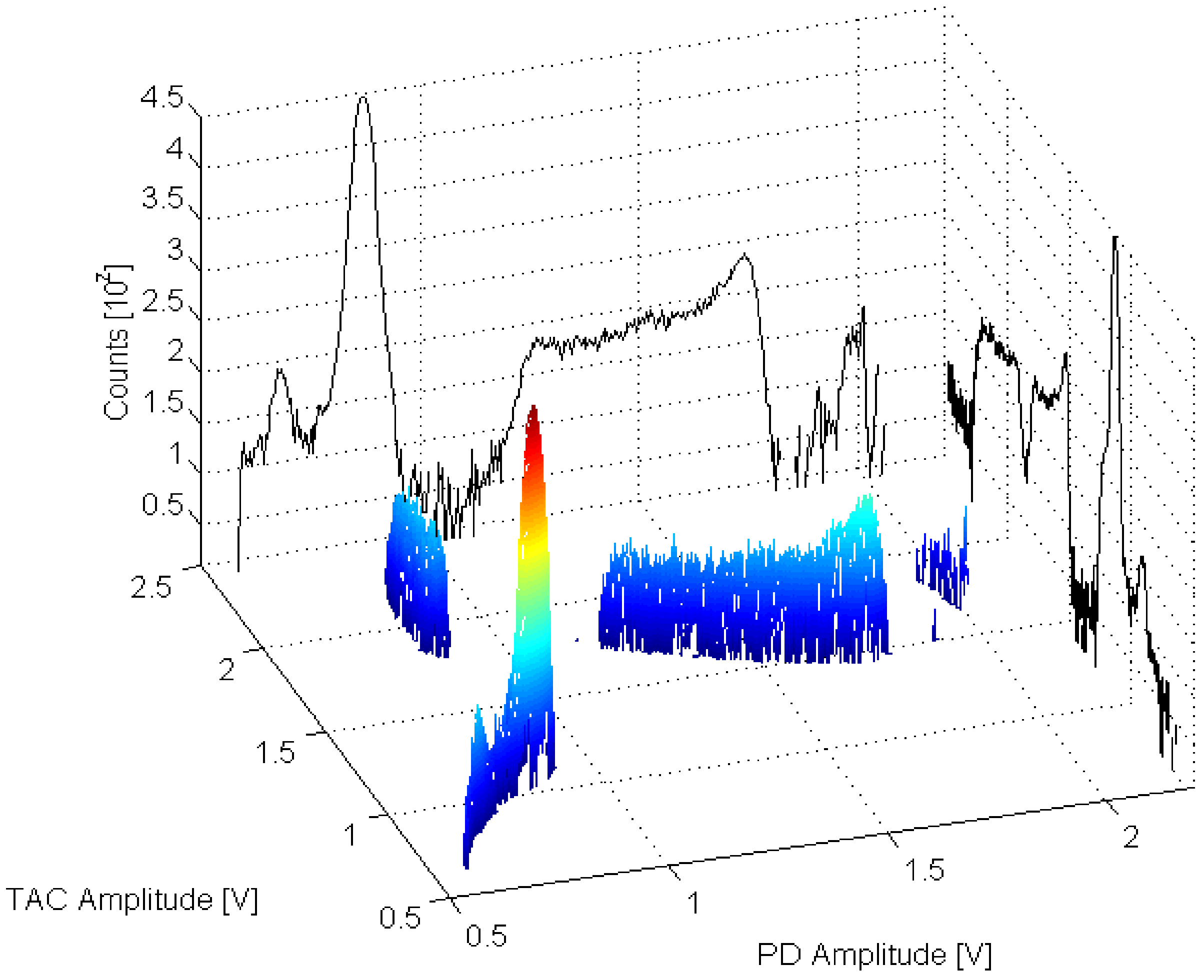
PDD Layout



size : 3.6 x 3.2 mm²
technology: 0.35µm CMOS
DP4M

Time-Over-Threshold Measurement for pile-up rejection

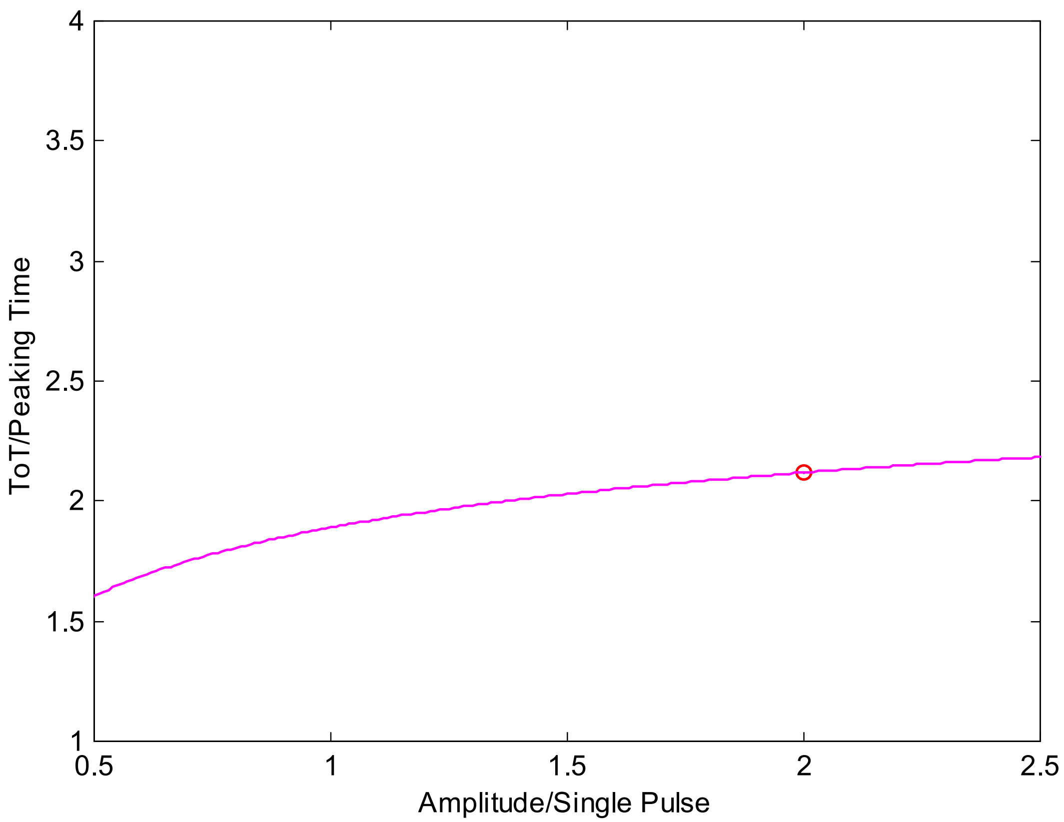
3D Pulse Height Spectrum as a function of the ToT



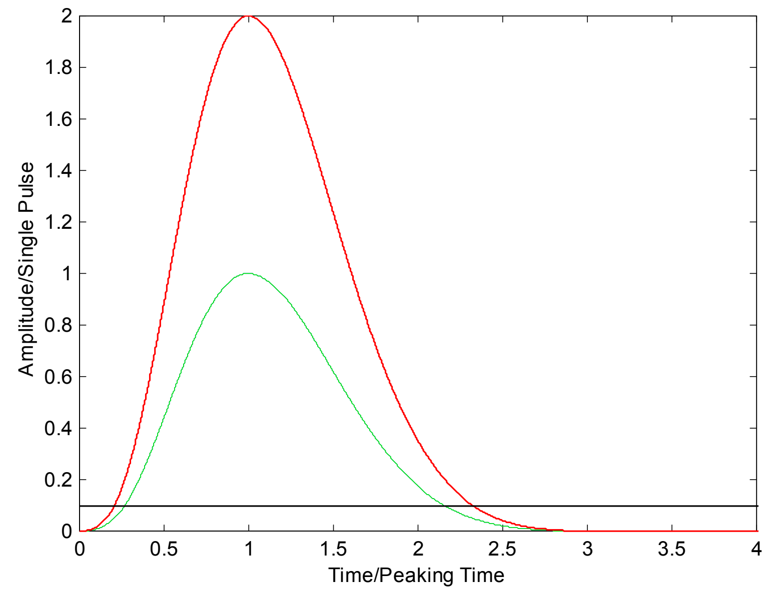
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



Delay = 0.0



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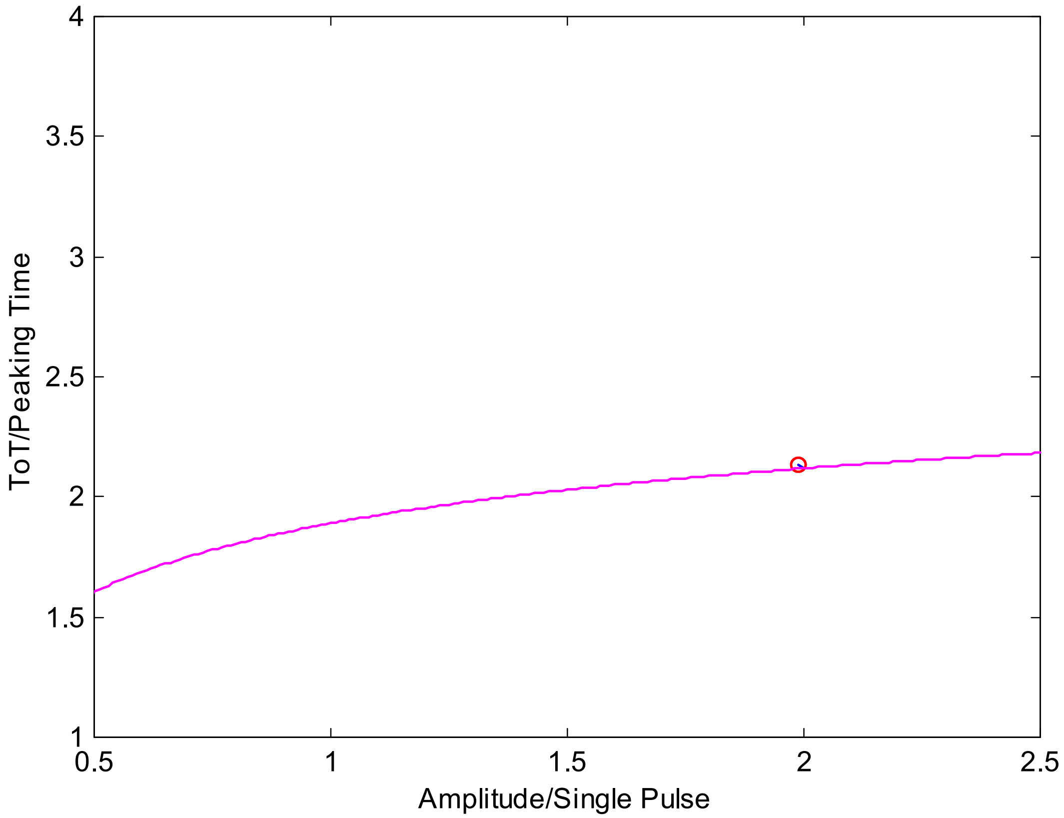
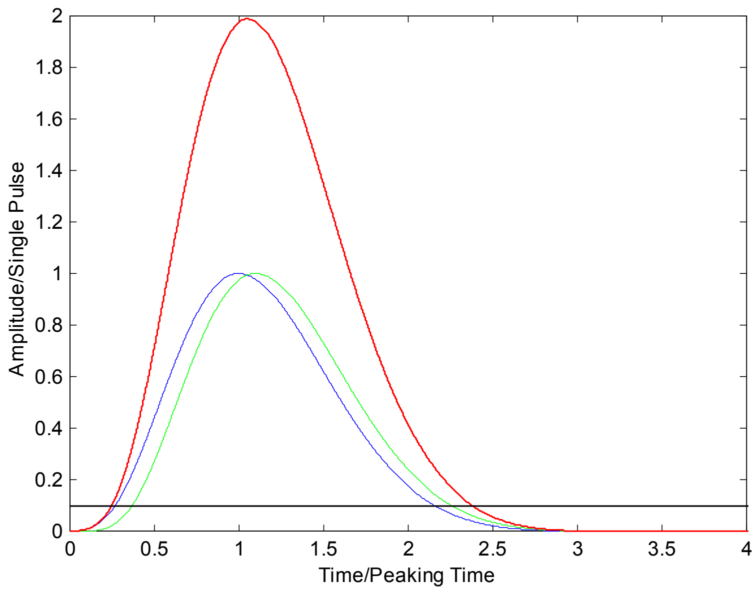


Delay = 0.1



Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

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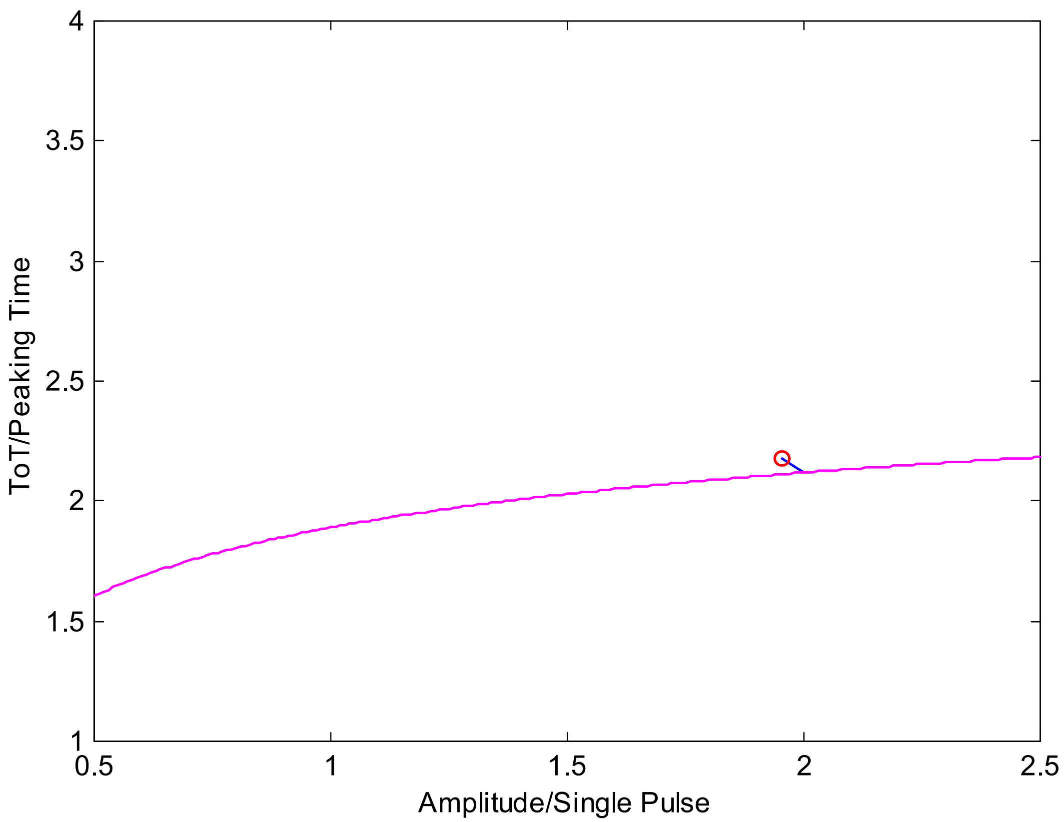
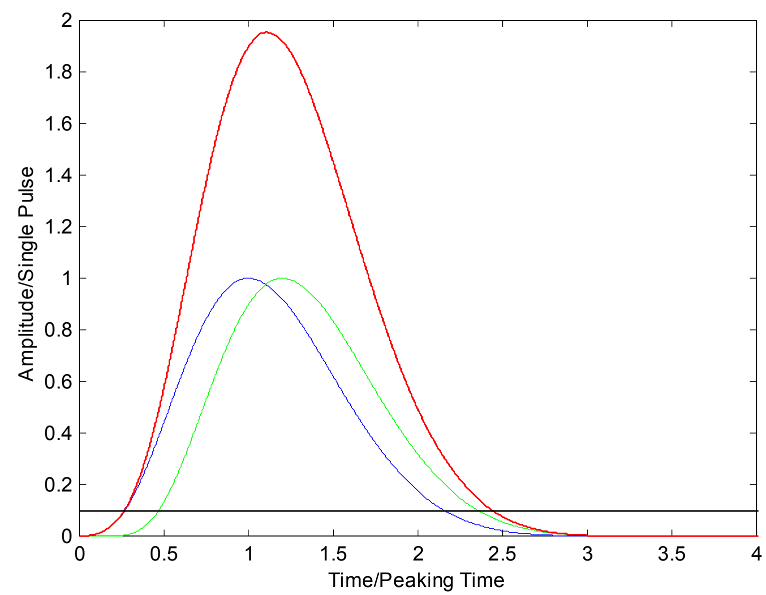


Delay = 0.2



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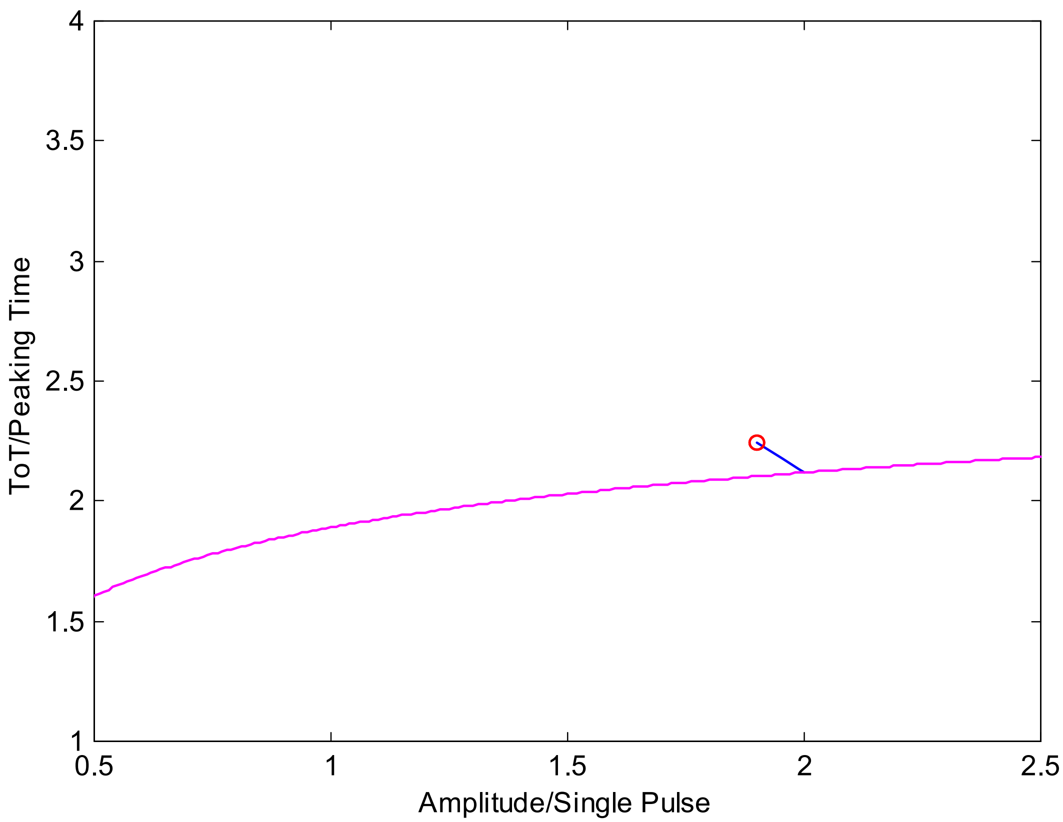
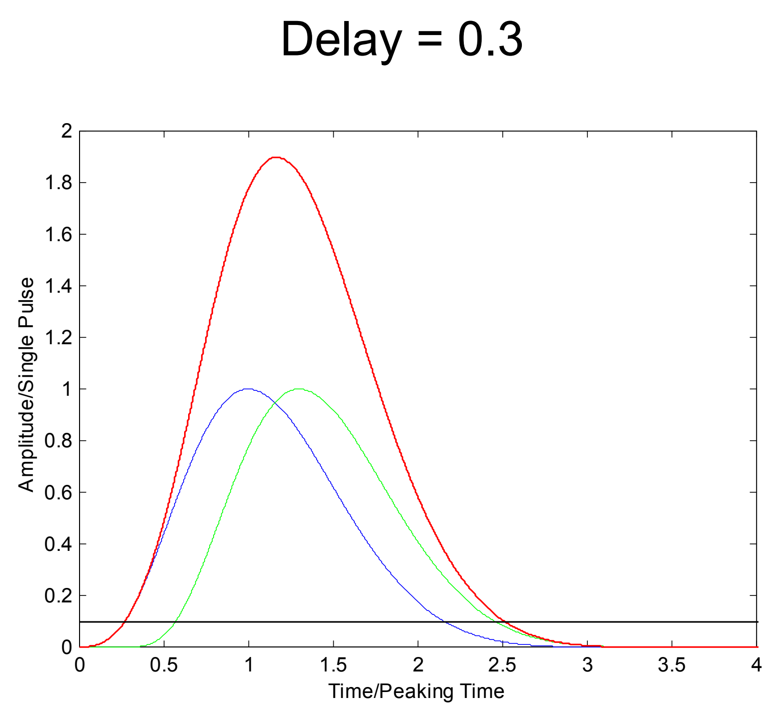
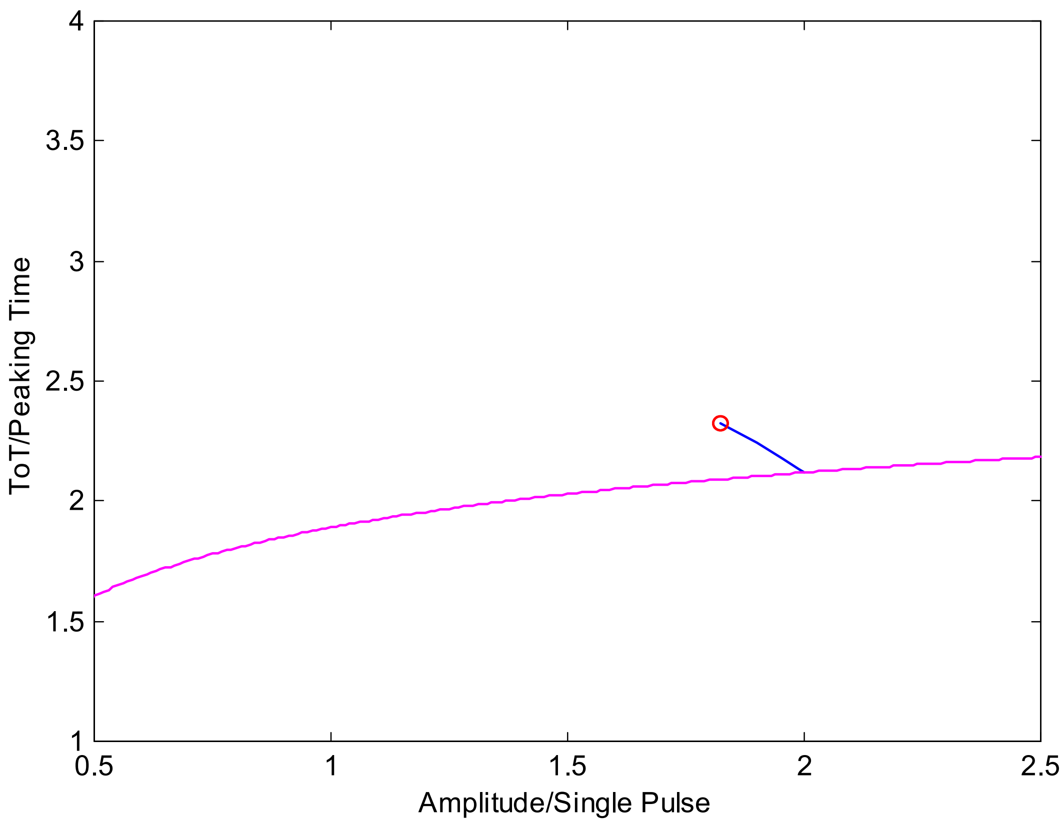




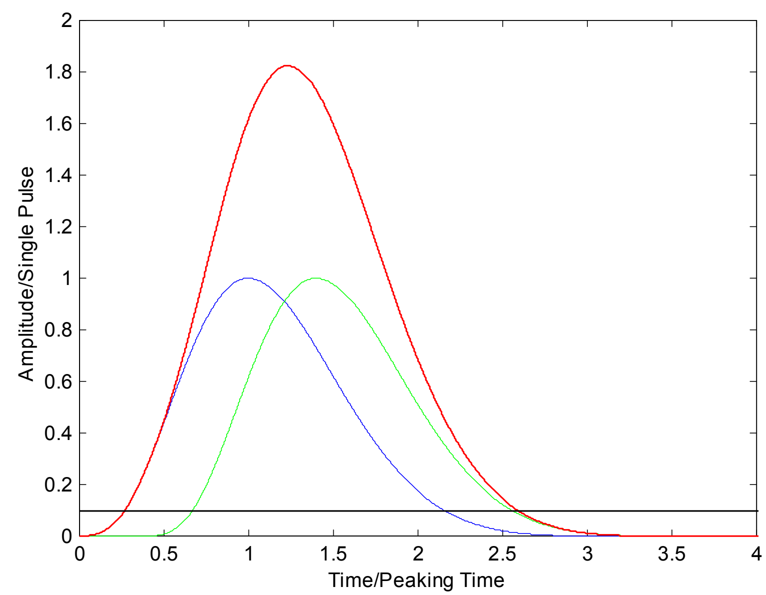
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



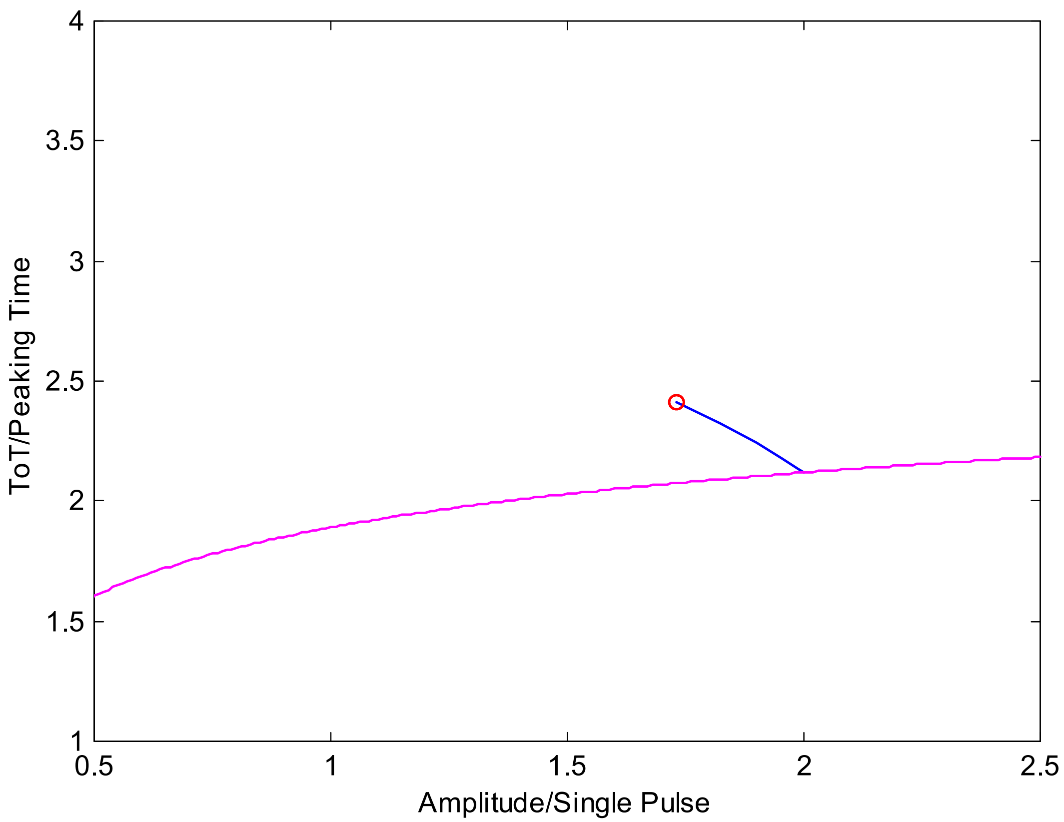
Delay = 0.4



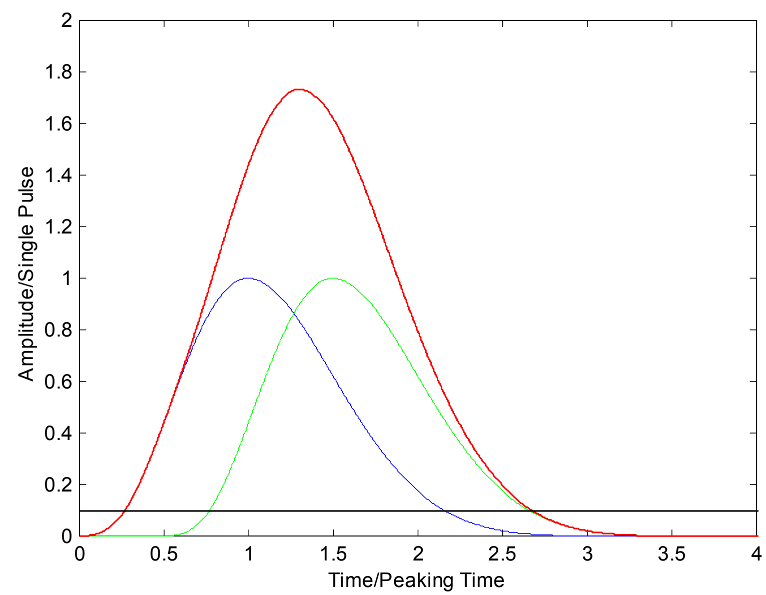
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



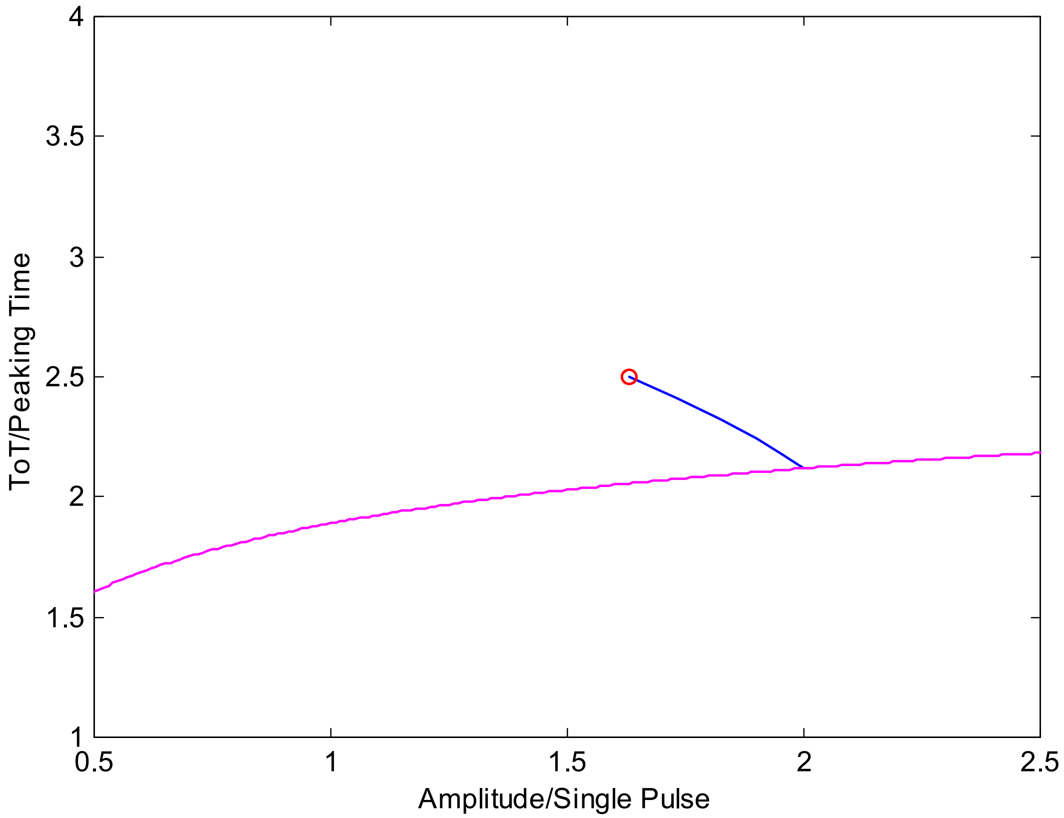
Delay = 0.5



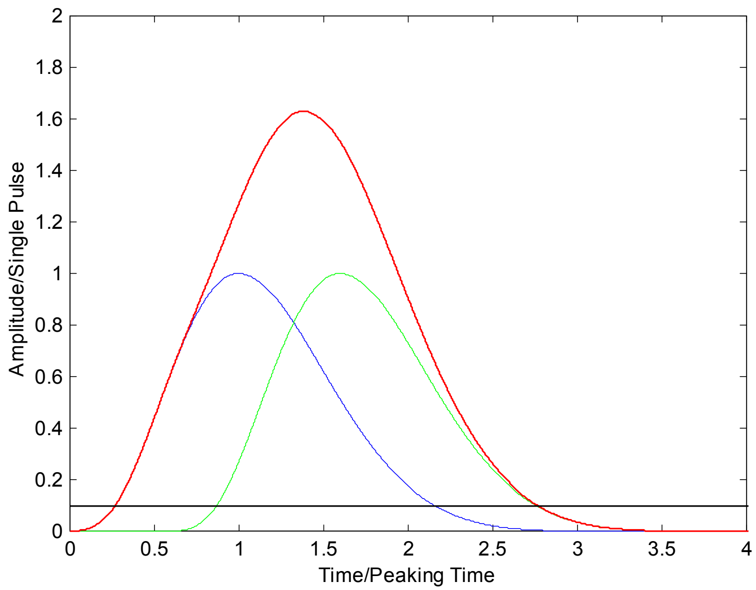
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



Delay = 0.6



Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

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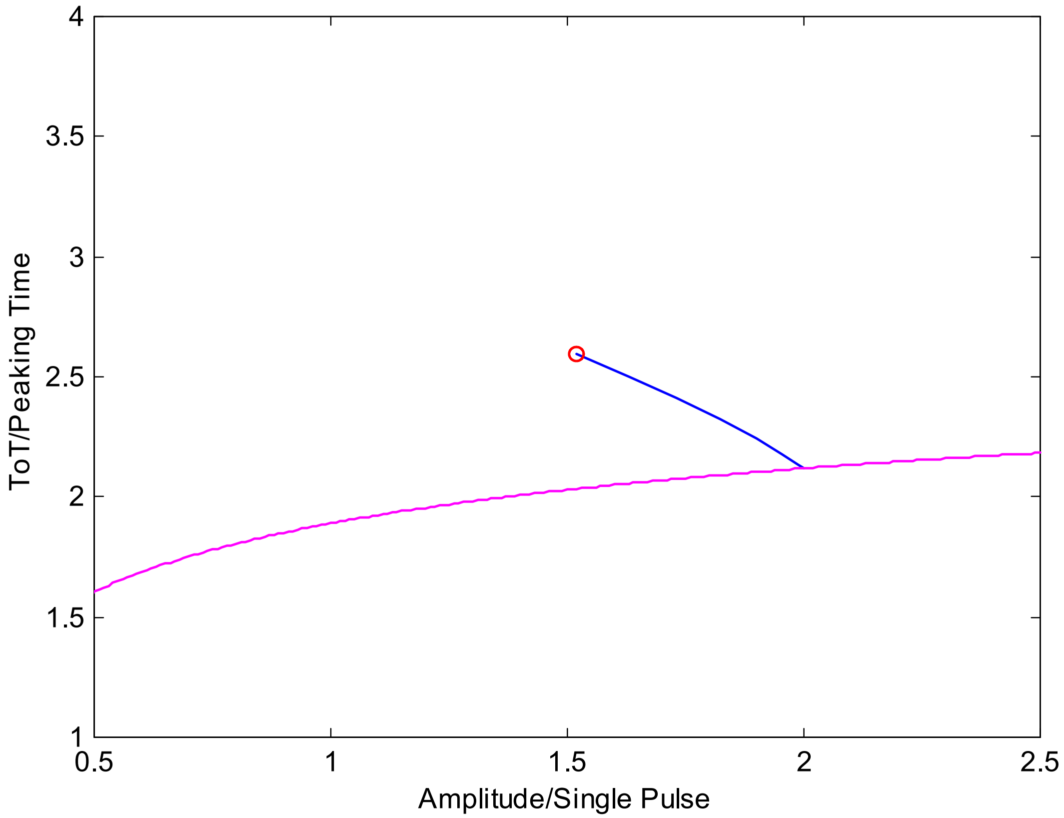
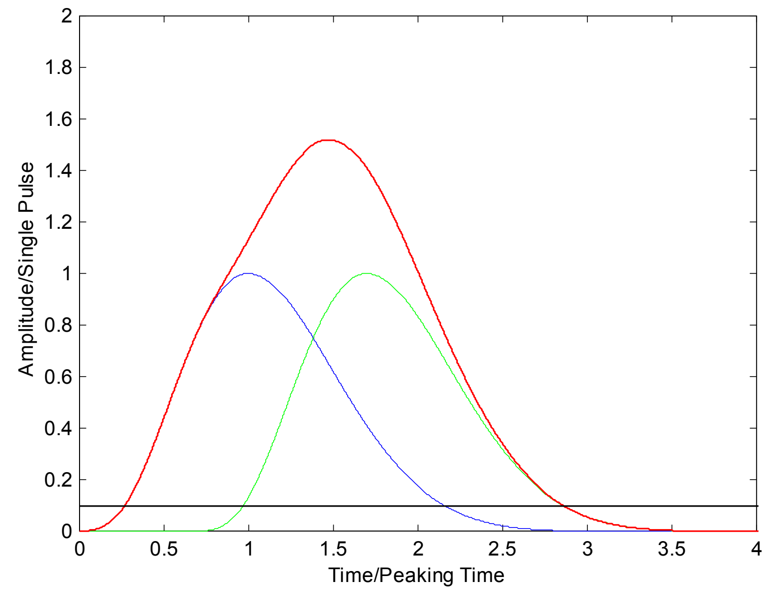


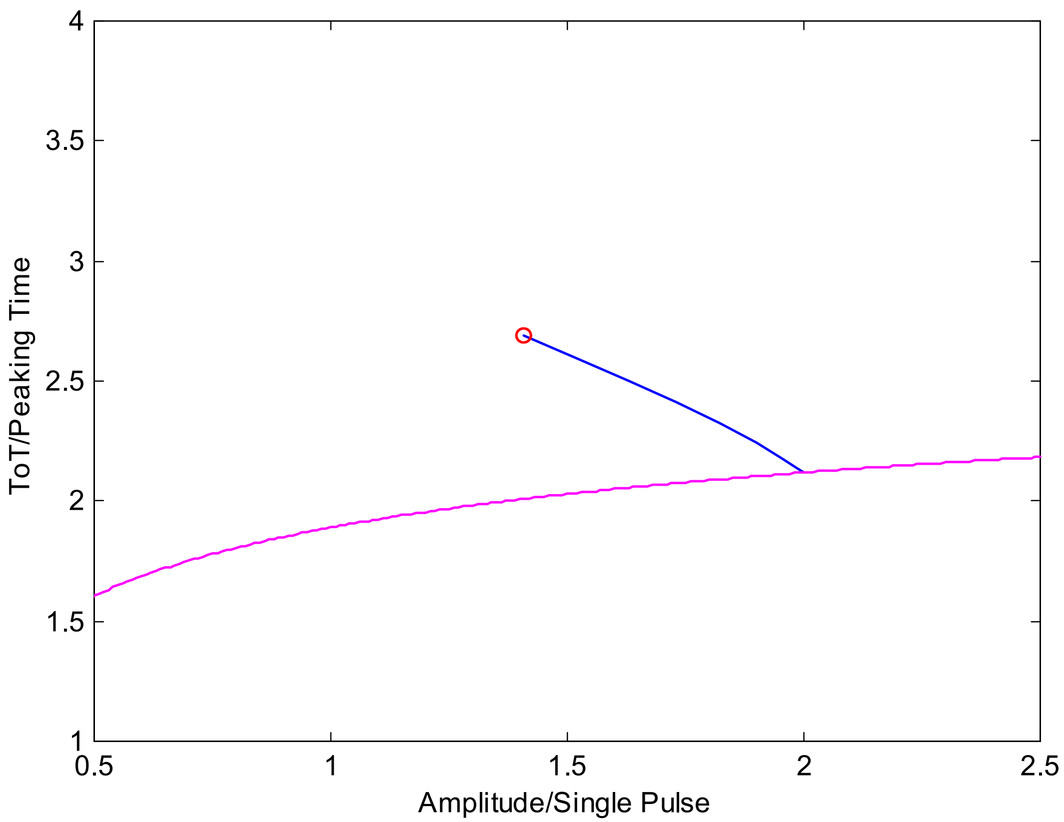
Delay = 0.7



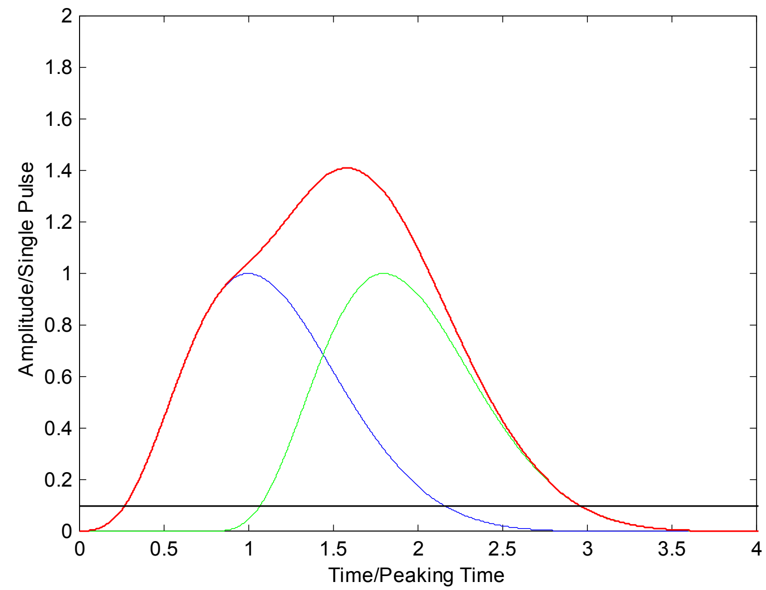
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5^{th} order complex poles semi-Gaussian shaper



Delay = 0.8



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U.S. Department of Energy

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Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

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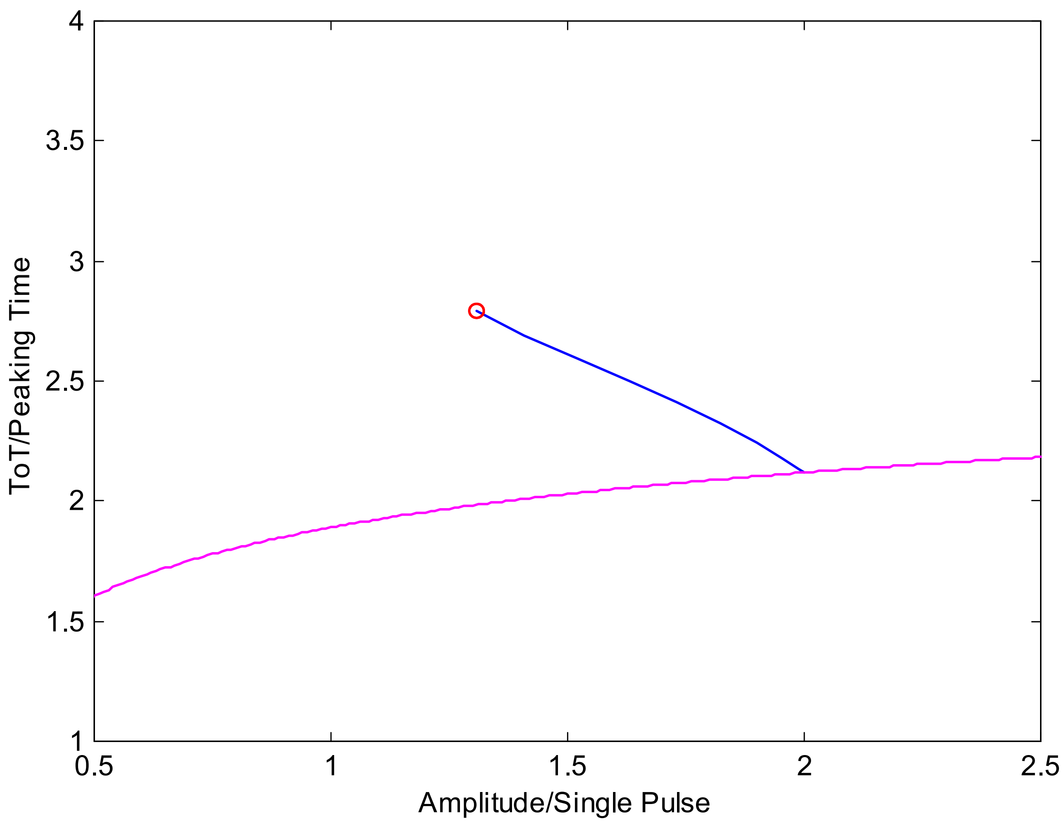
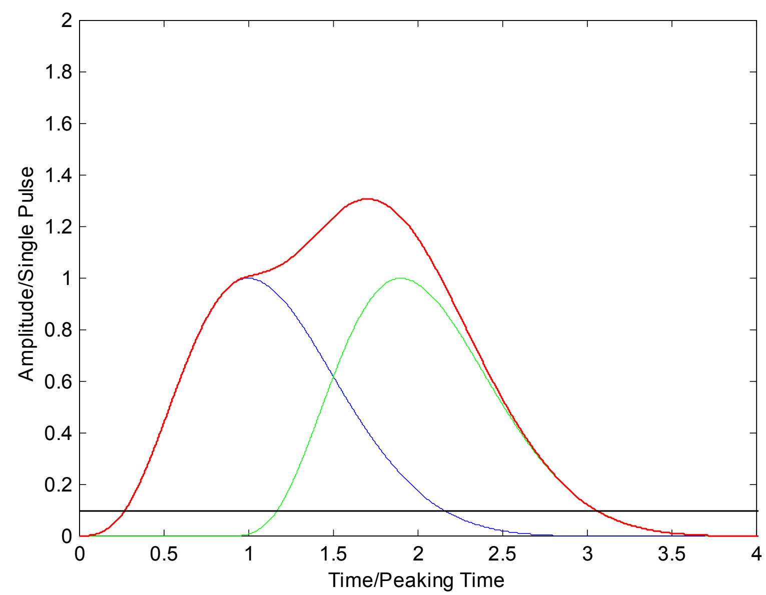


Delay = 0.9



Time-Over-Threshold Measurement for pile-up rejection

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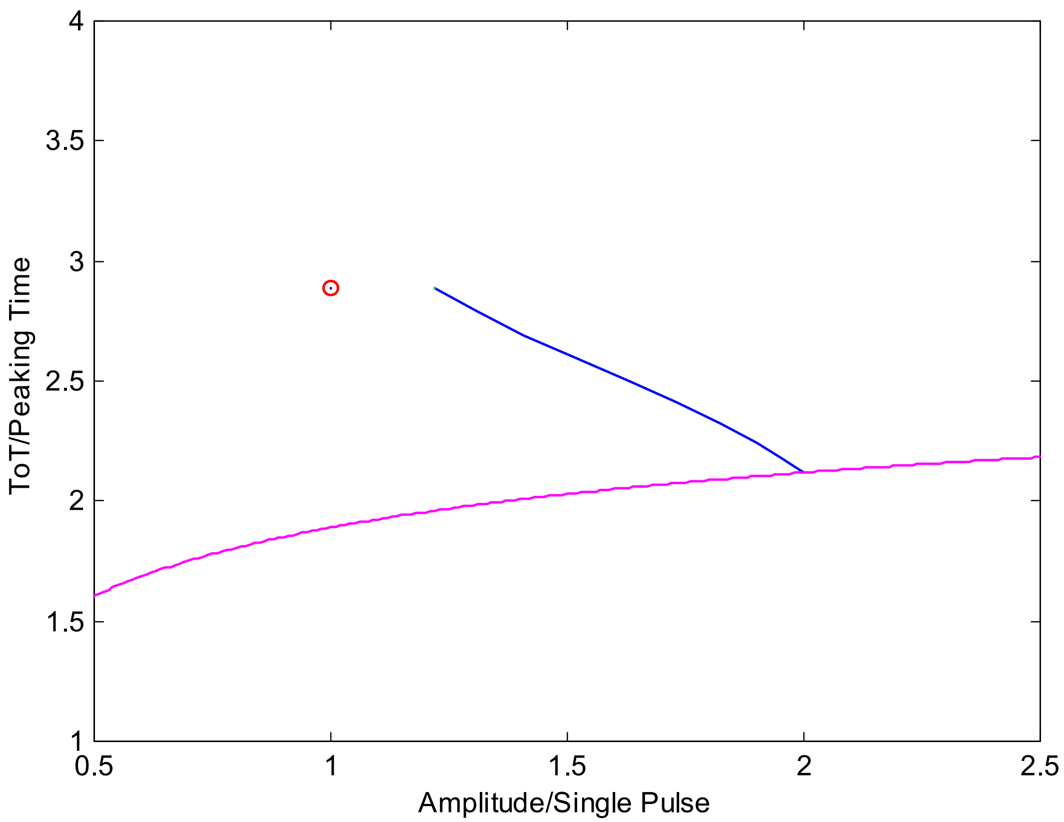
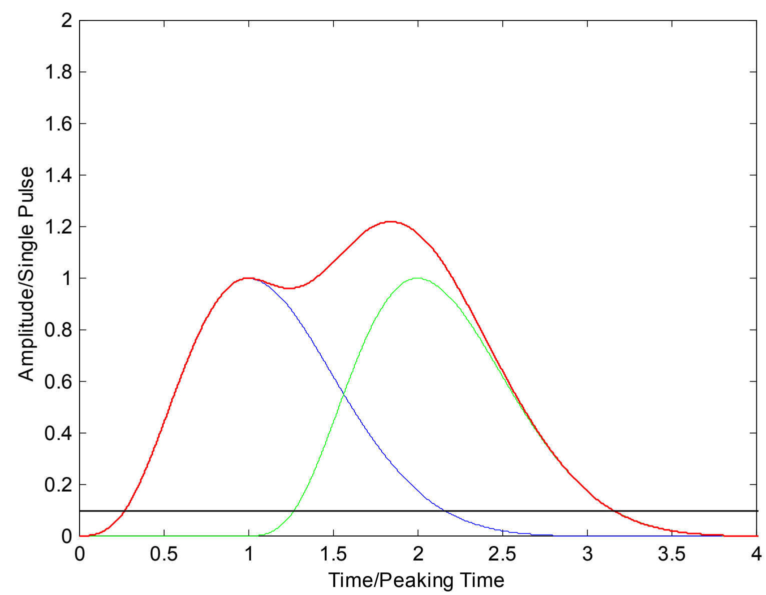


Delay = 1.0



Time-Over-Threshold Measurement for pile-up rejection

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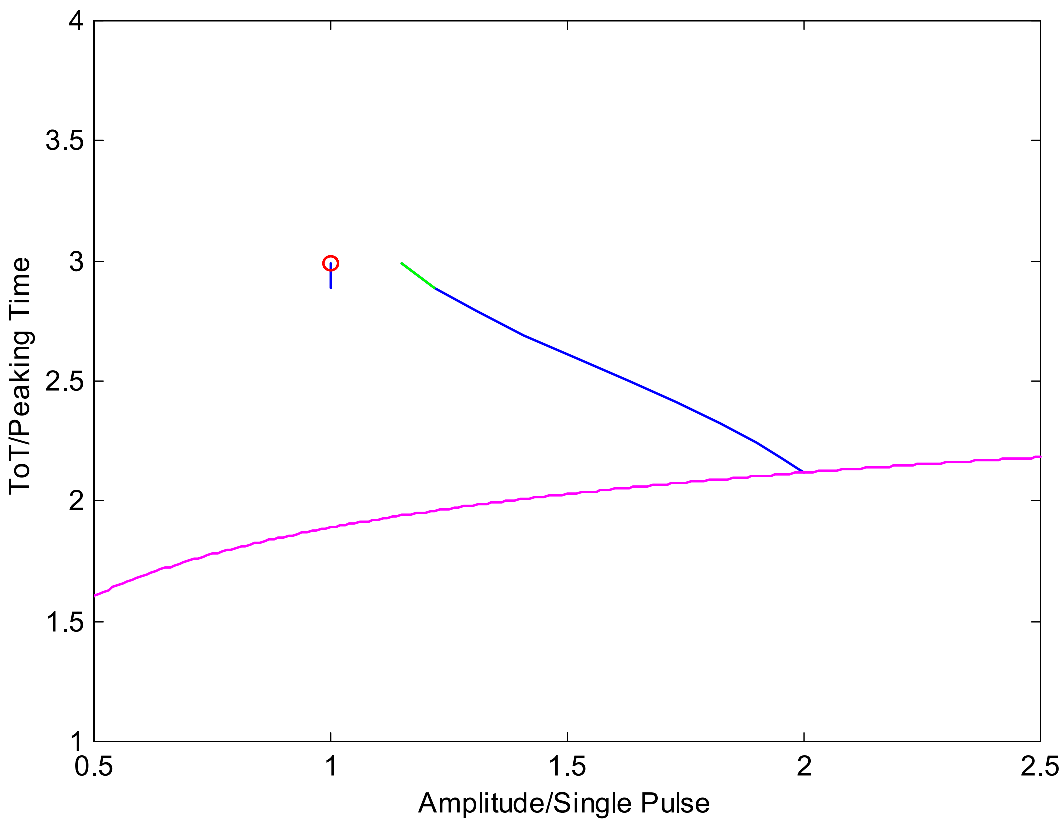
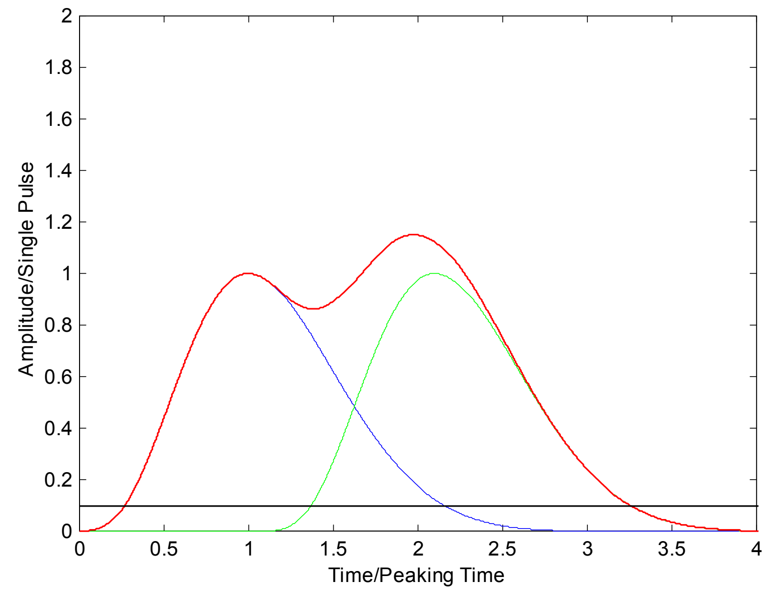


Delay = 1.1



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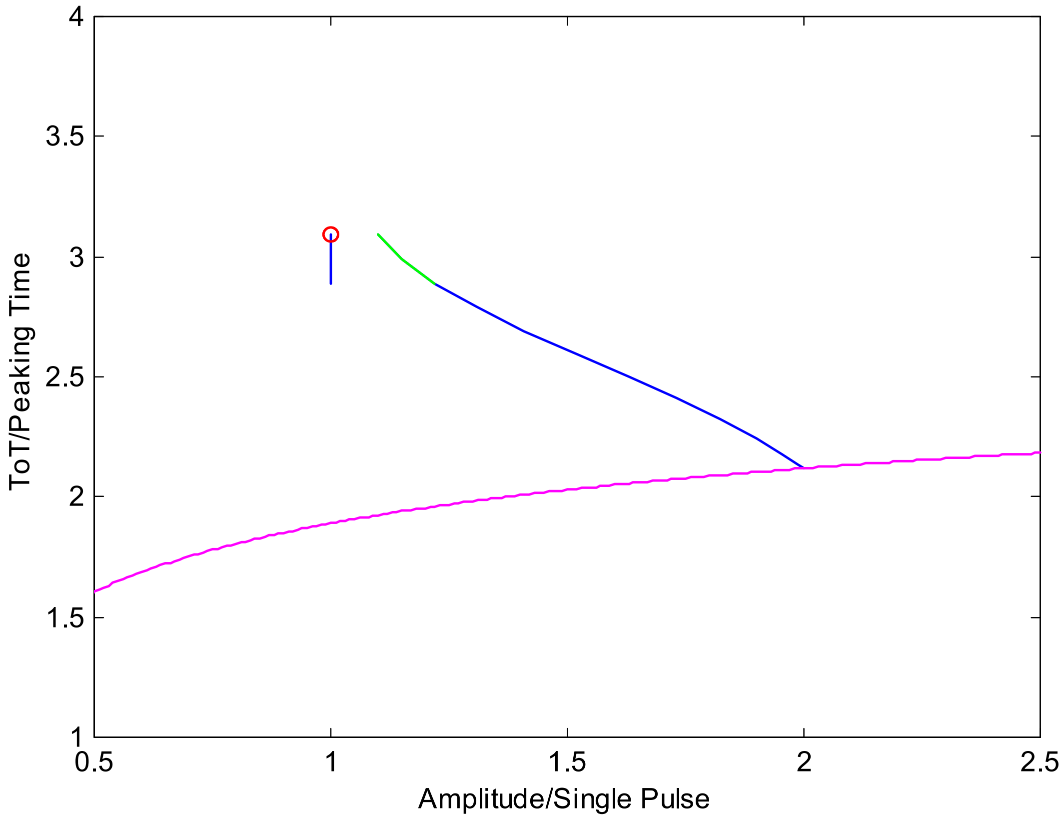
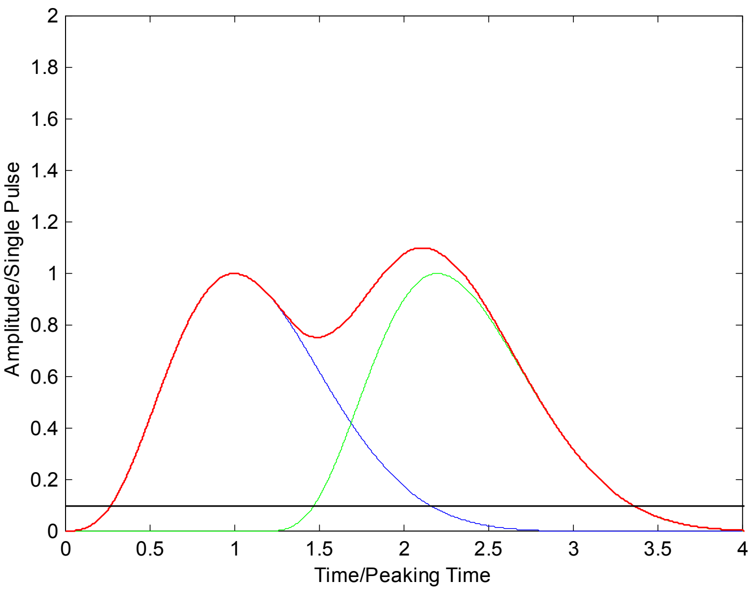


Delay = 1.2



Time-Over-Threshold Measurement for pile-up rejection

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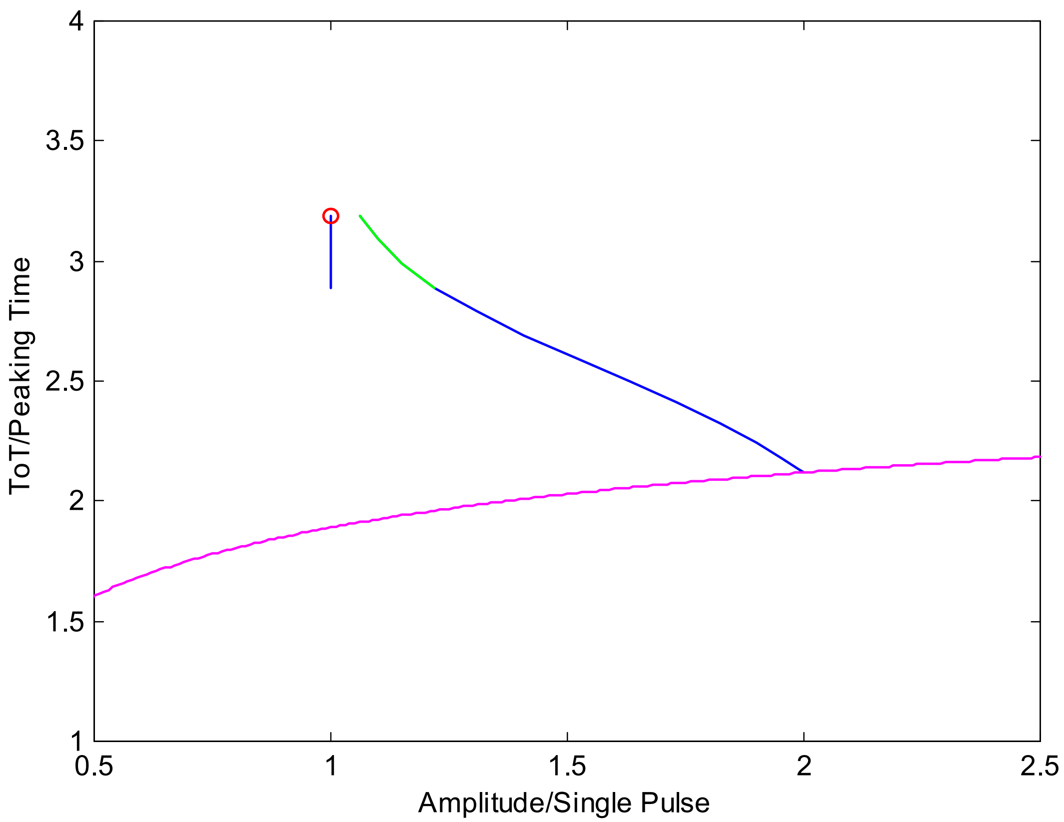
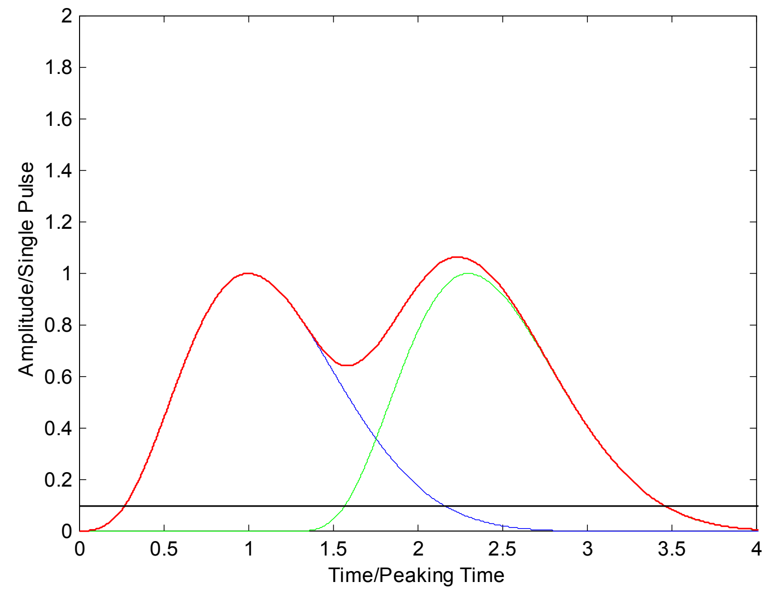


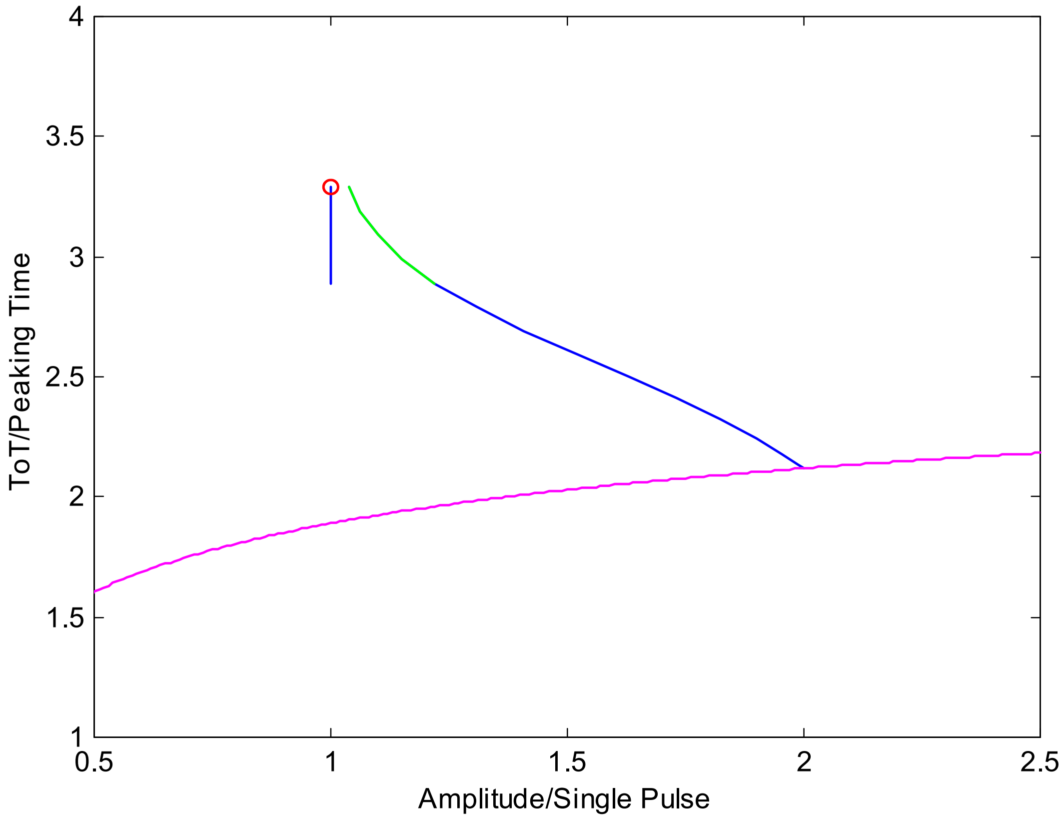
Delay = 1.3



Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



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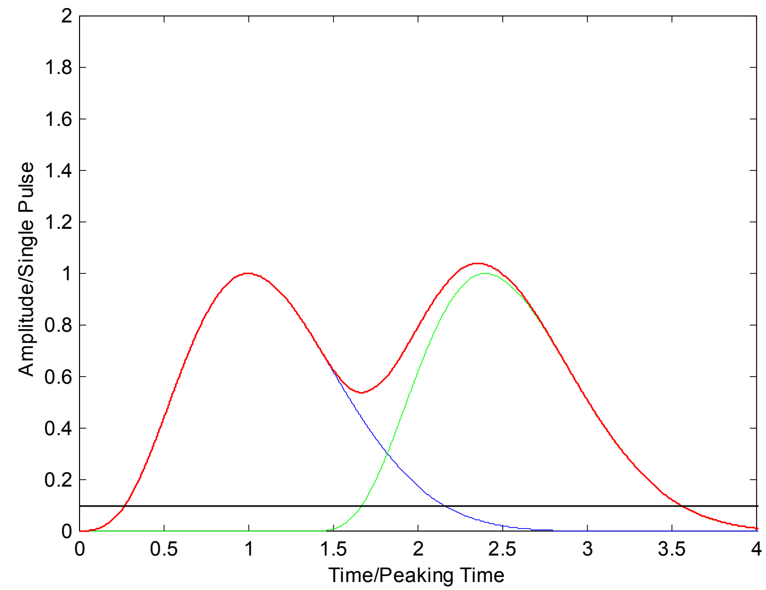

Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

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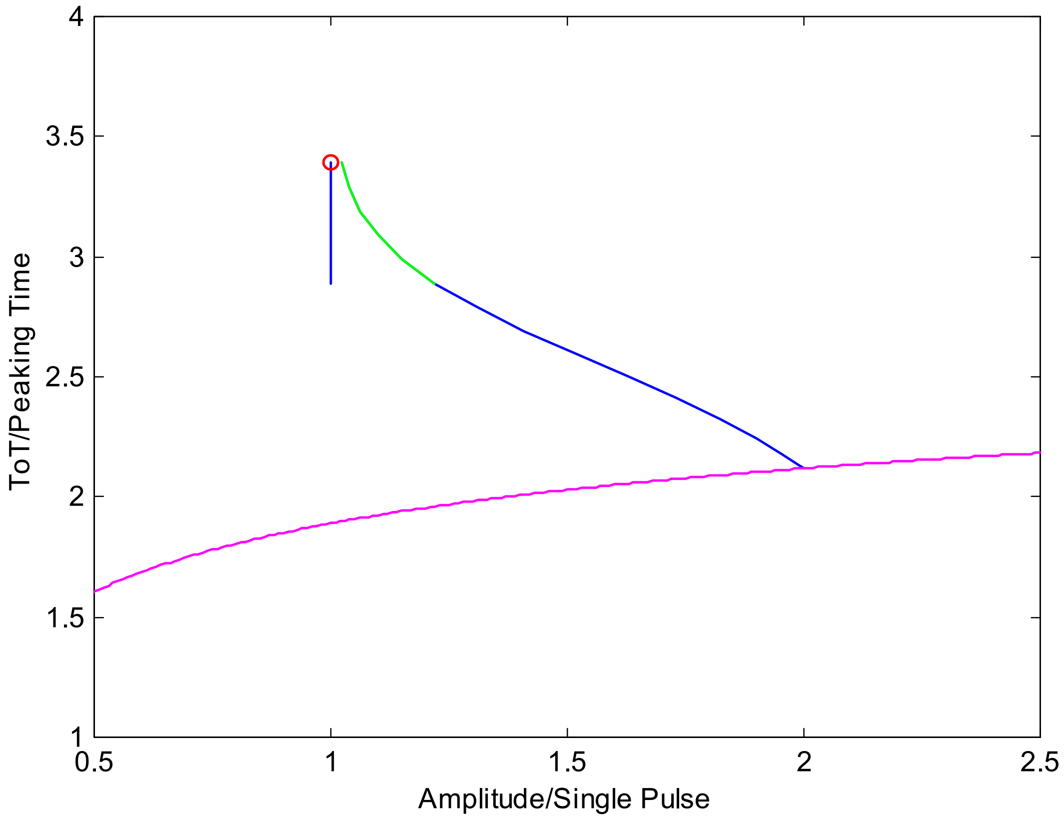

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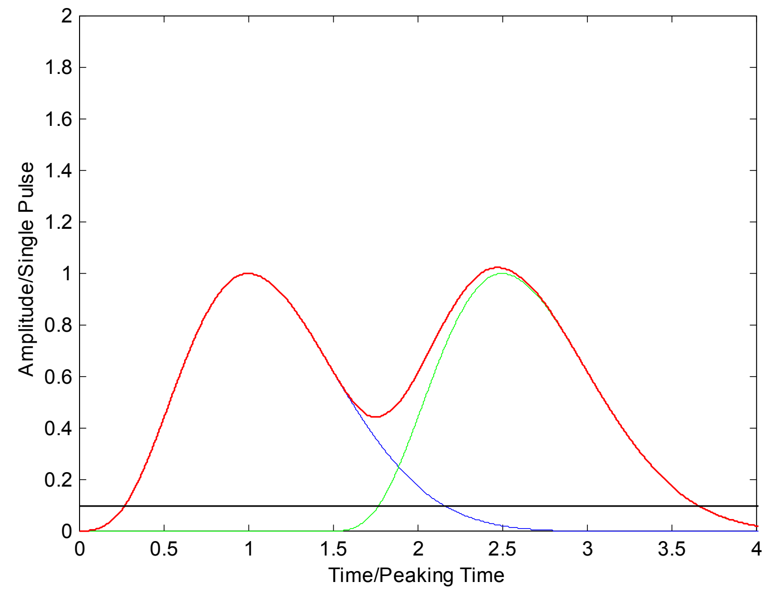
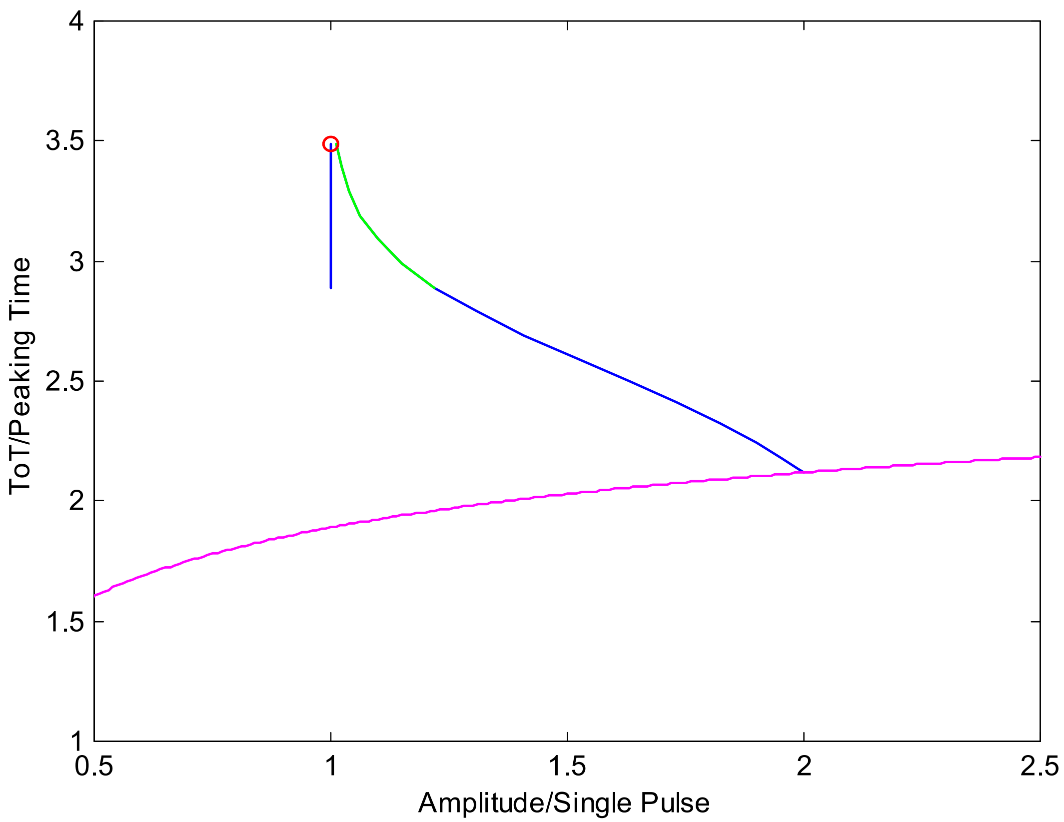


Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



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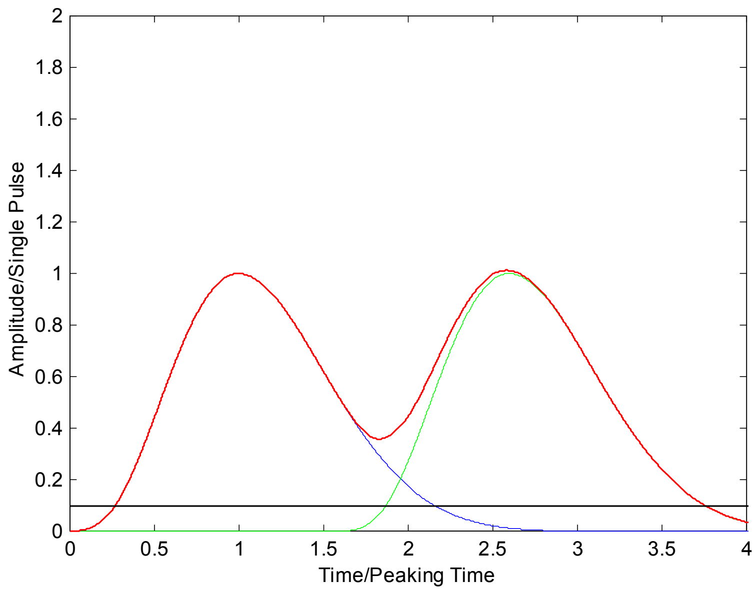

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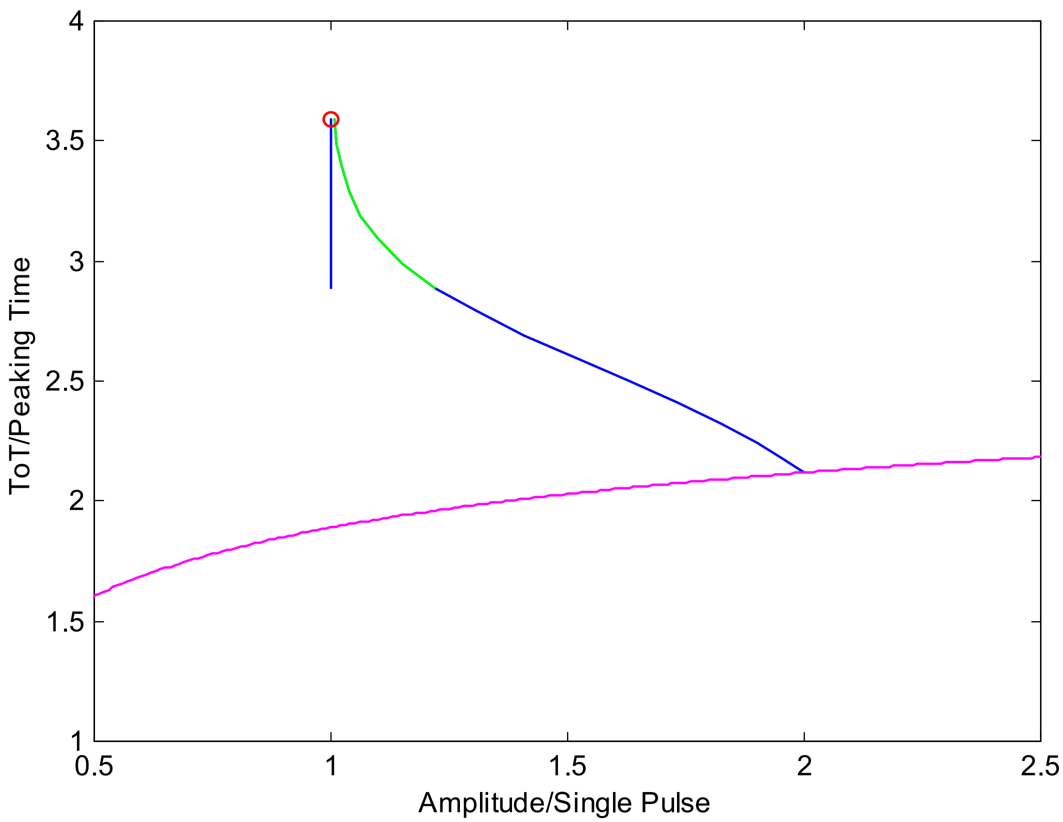
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



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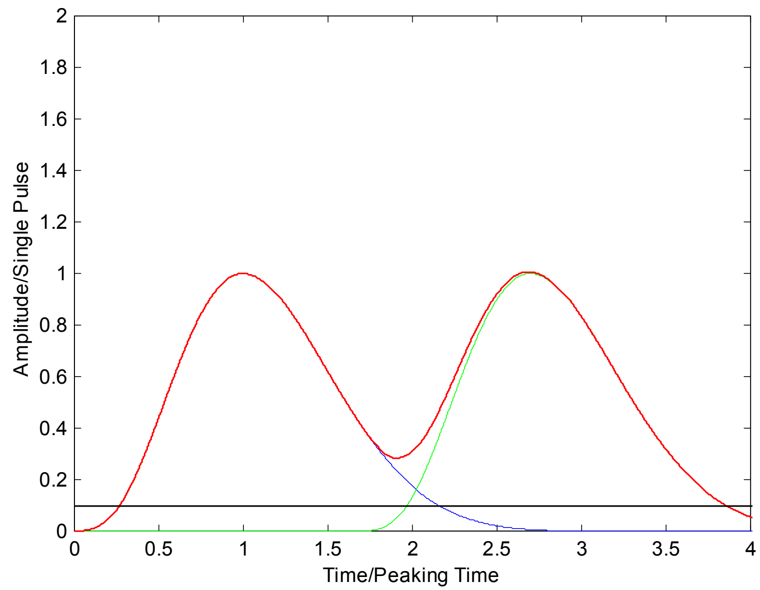
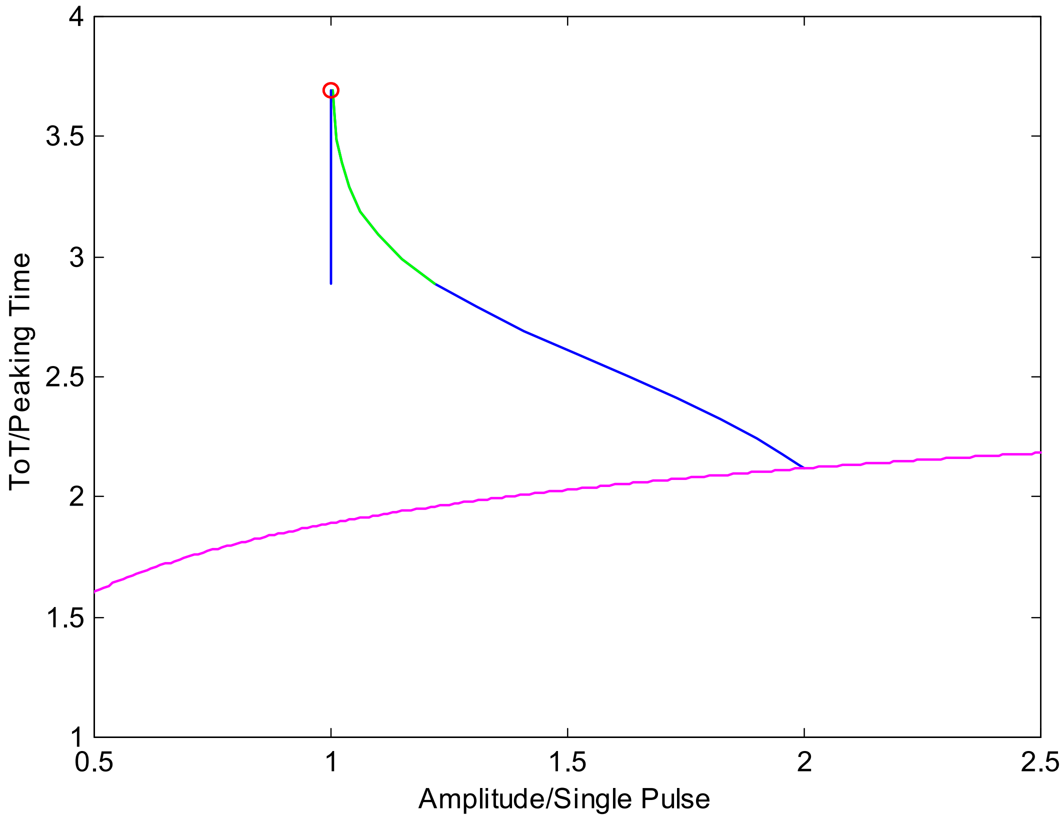


Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



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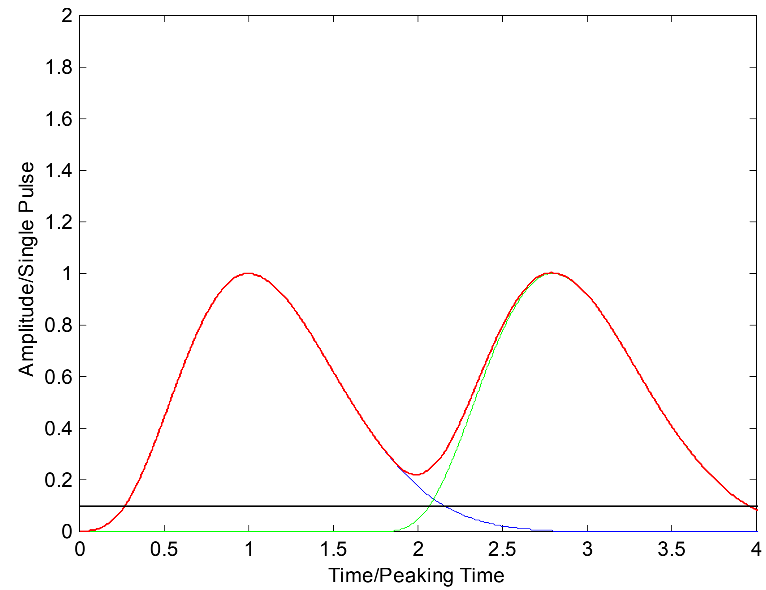

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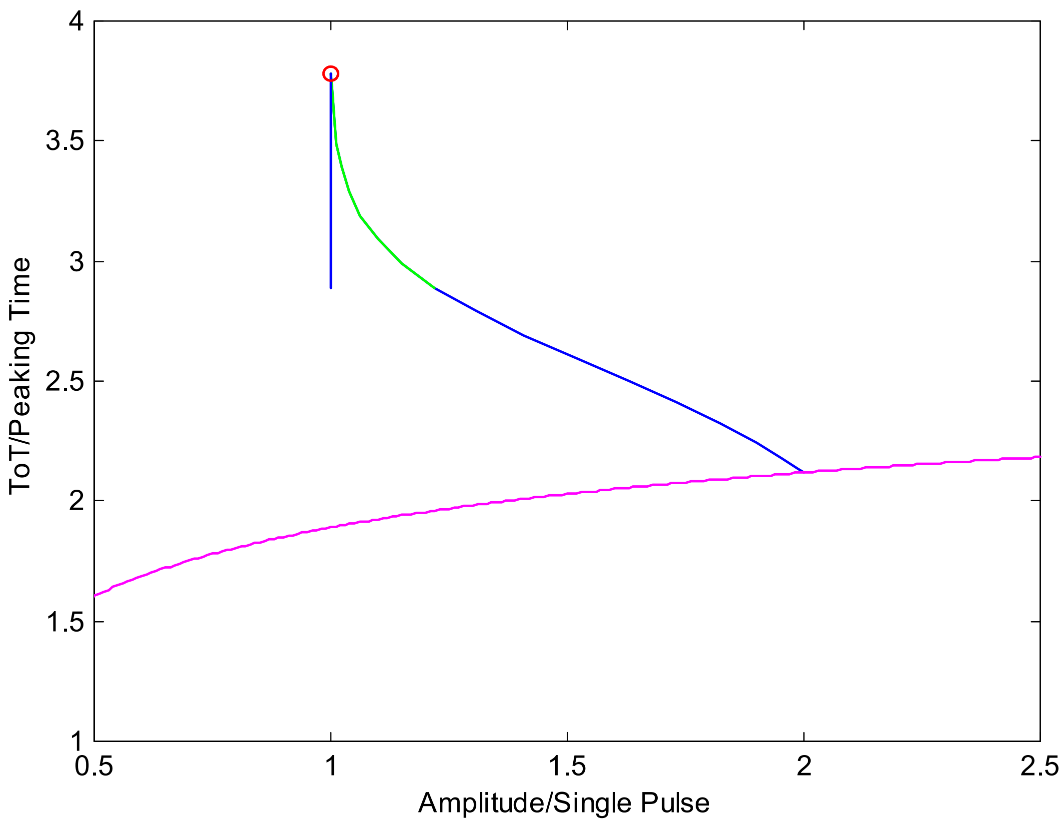
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



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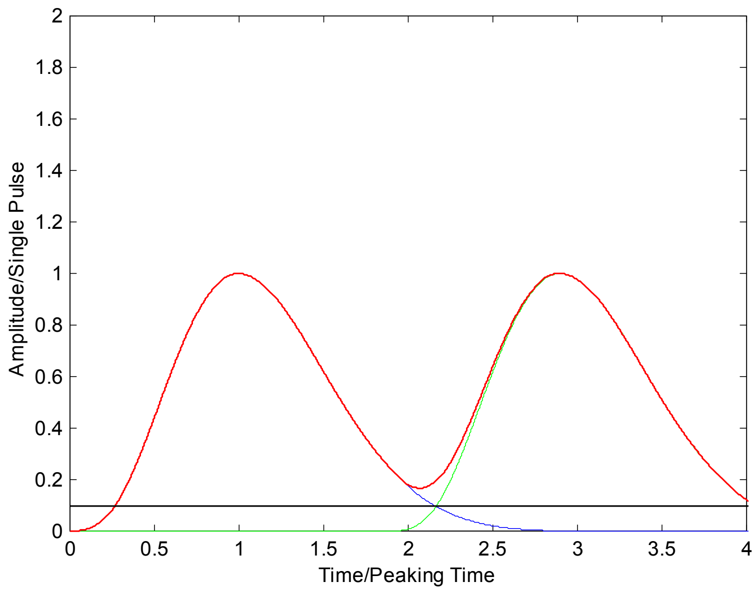
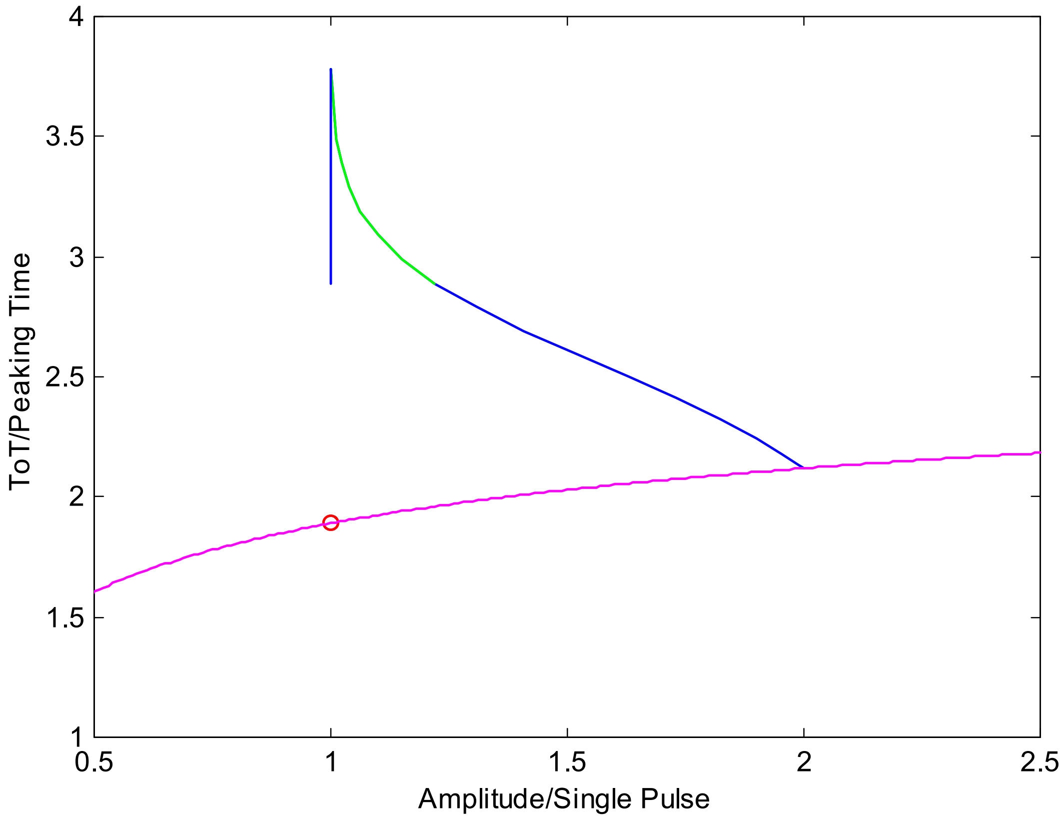


Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



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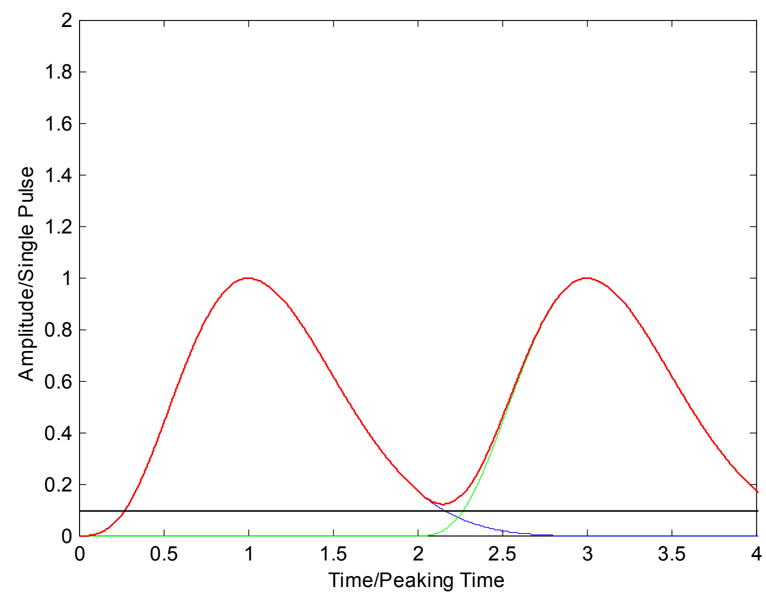
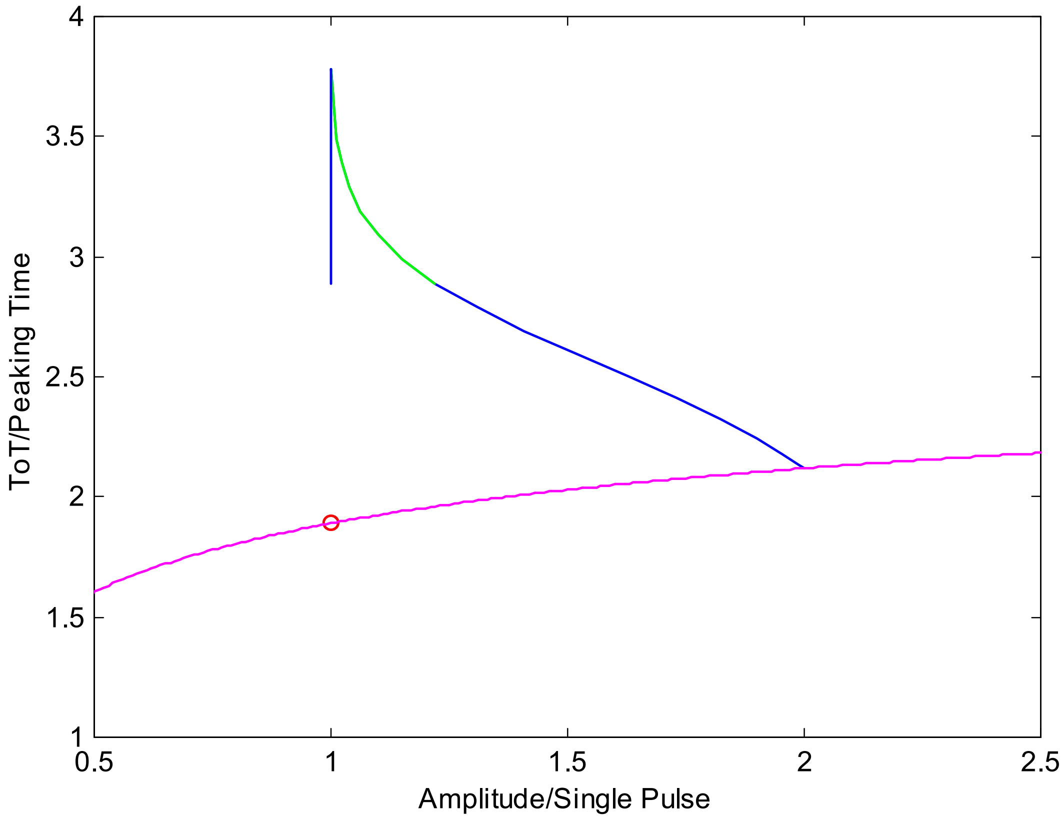


Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



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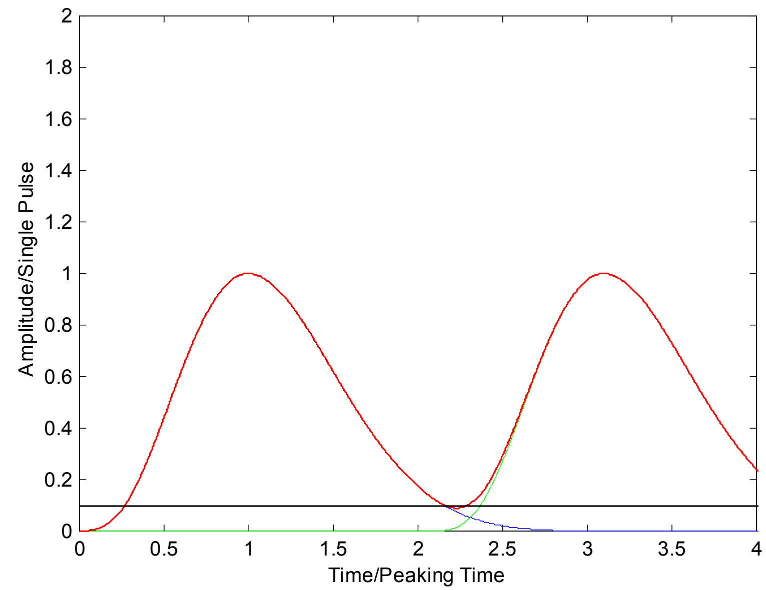
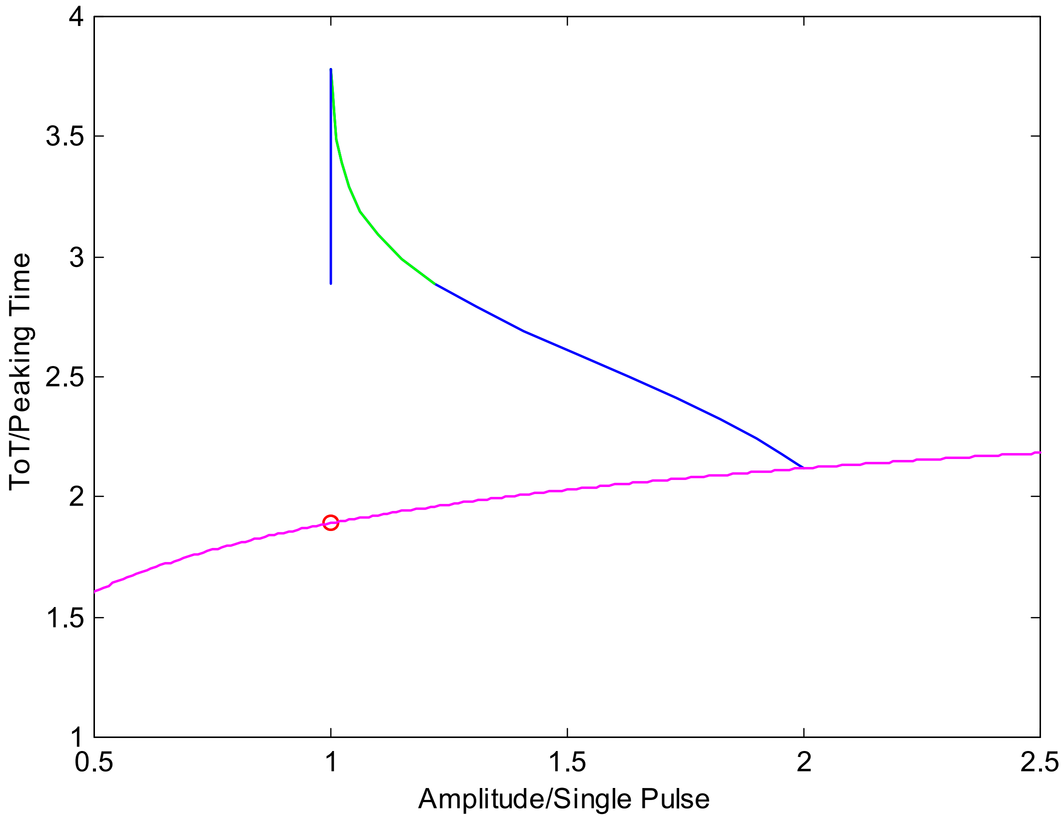


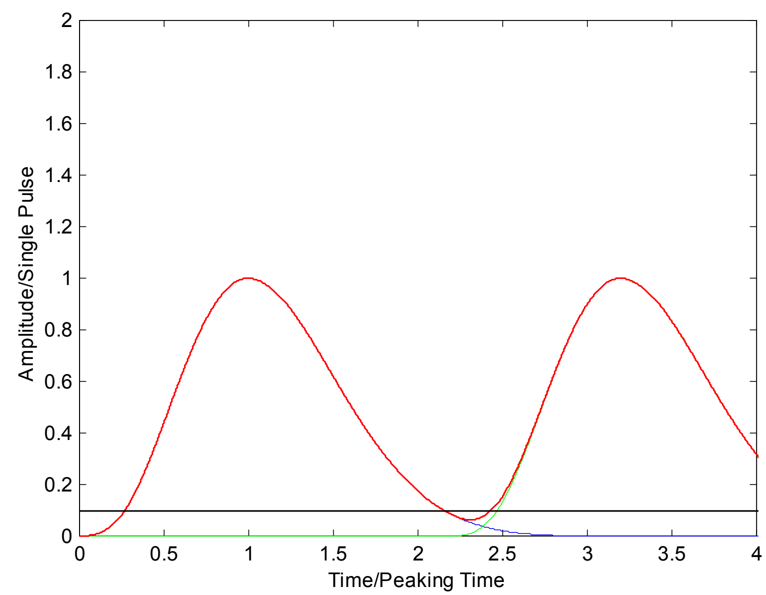
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



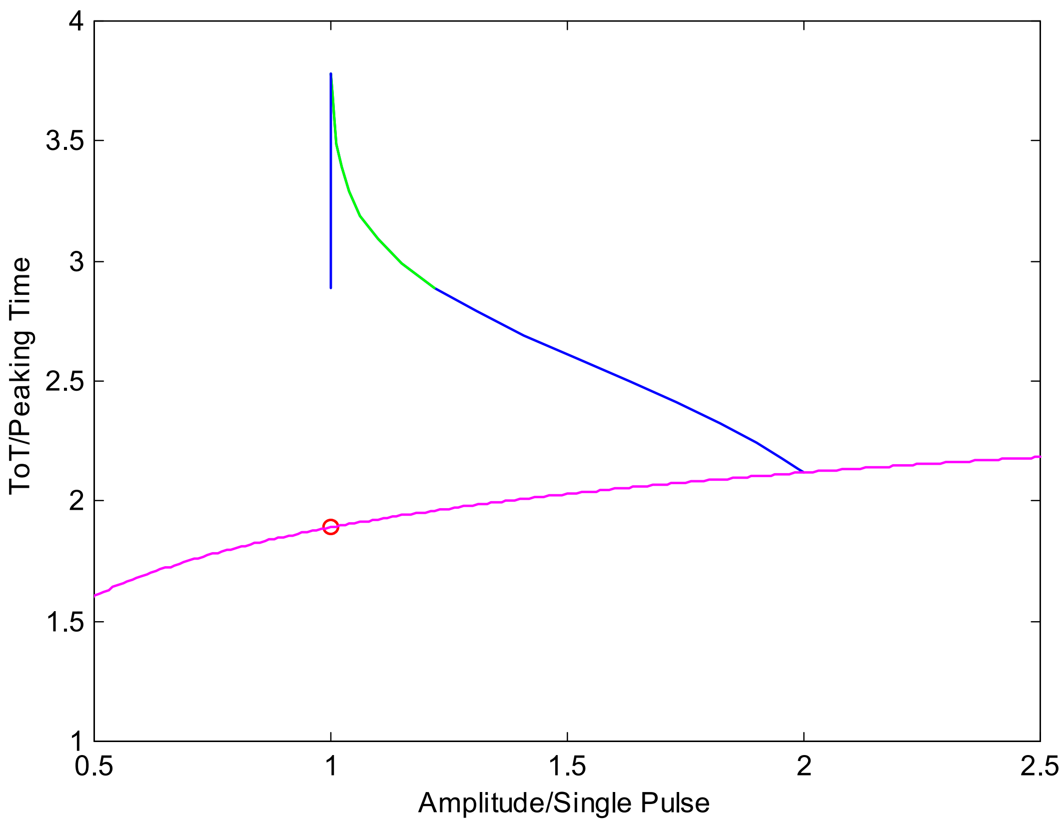
Delay = 2.2



Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



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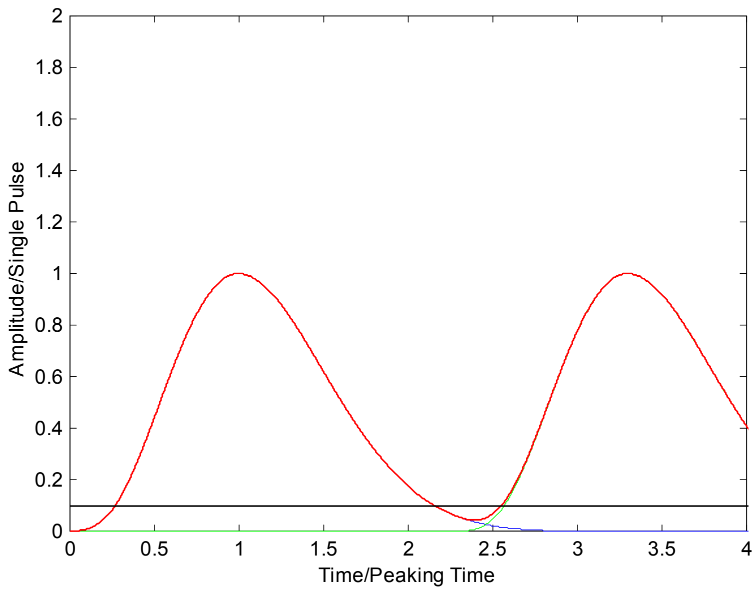
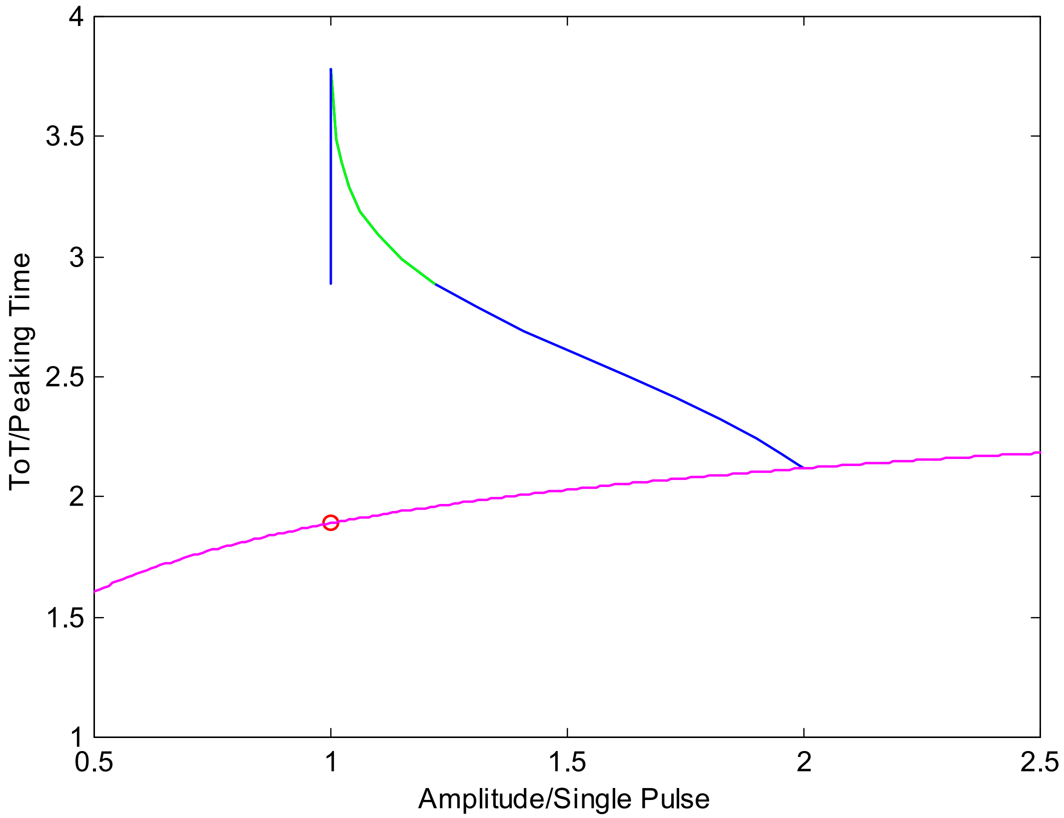


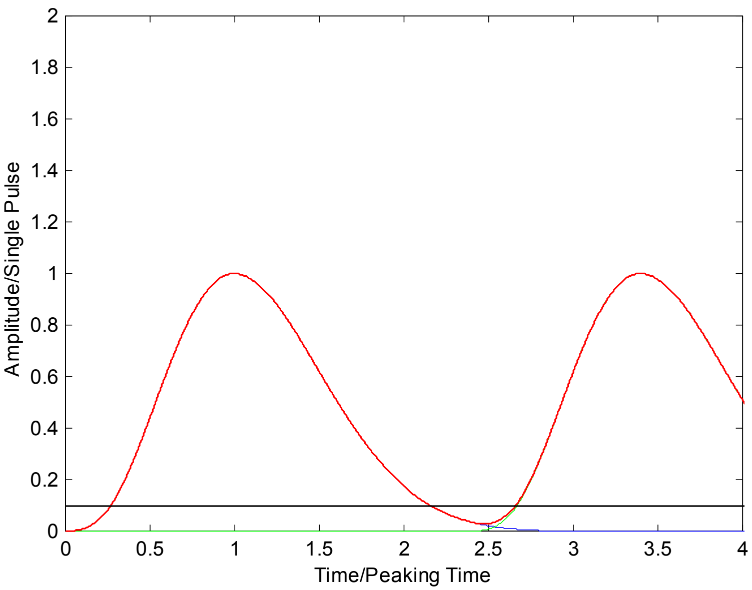
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper



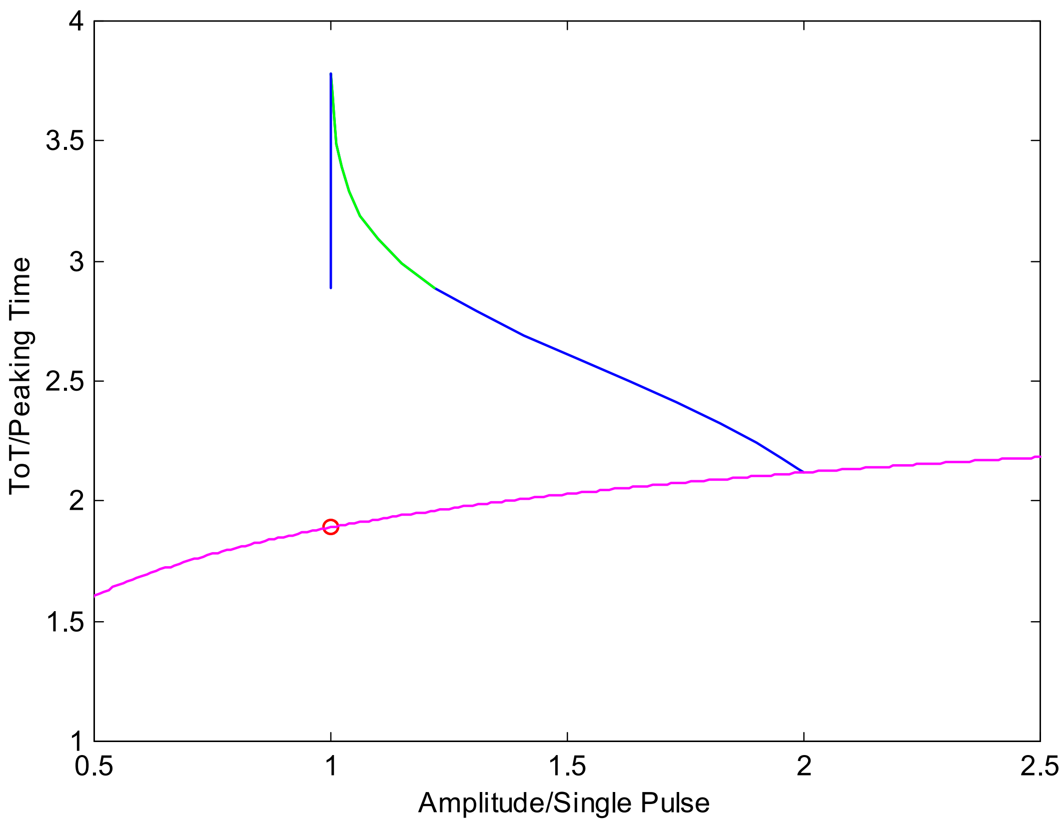
Delay = 2.4



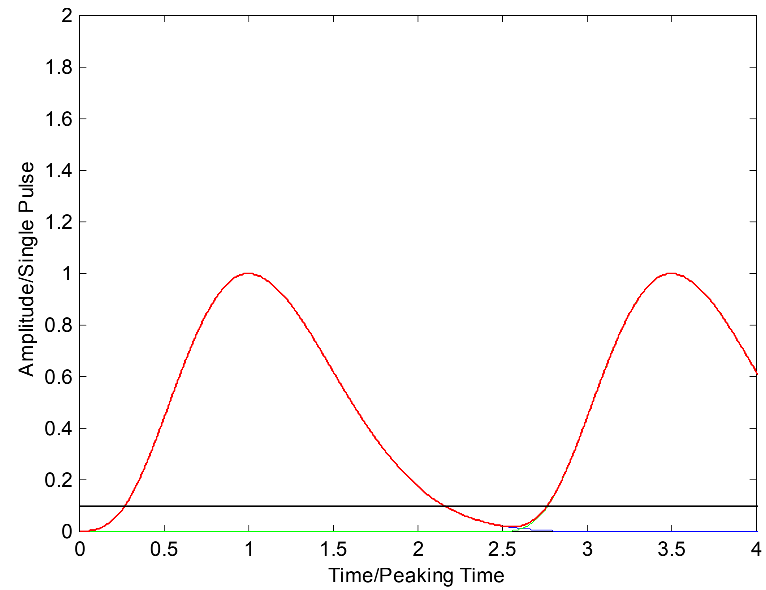
Time-Over-Threshold Measurement for pile-up rejection

ToT vs. Peak Amplitude Characteristic

for a pulse from a 5th order complex poles semi-Gaussian shaper

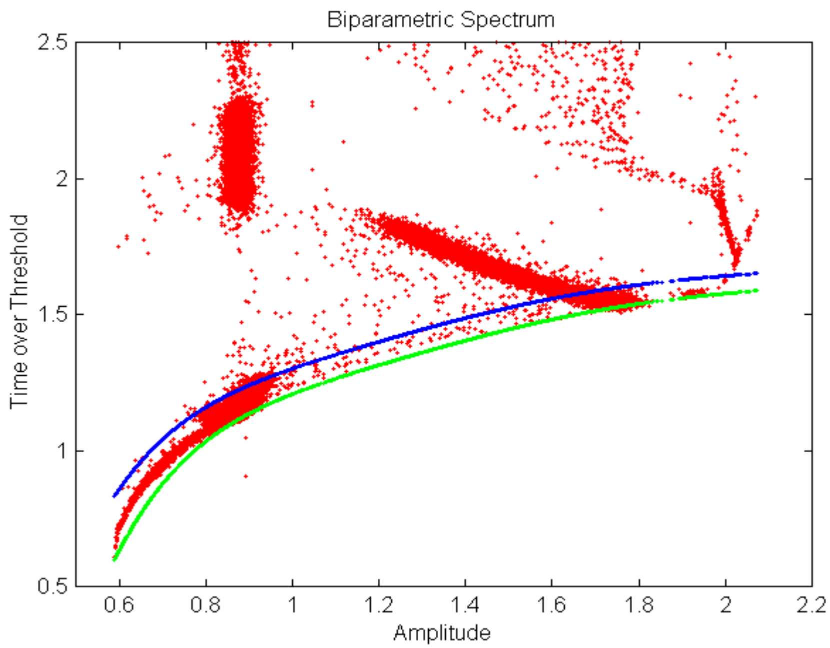


Delay = 2.5

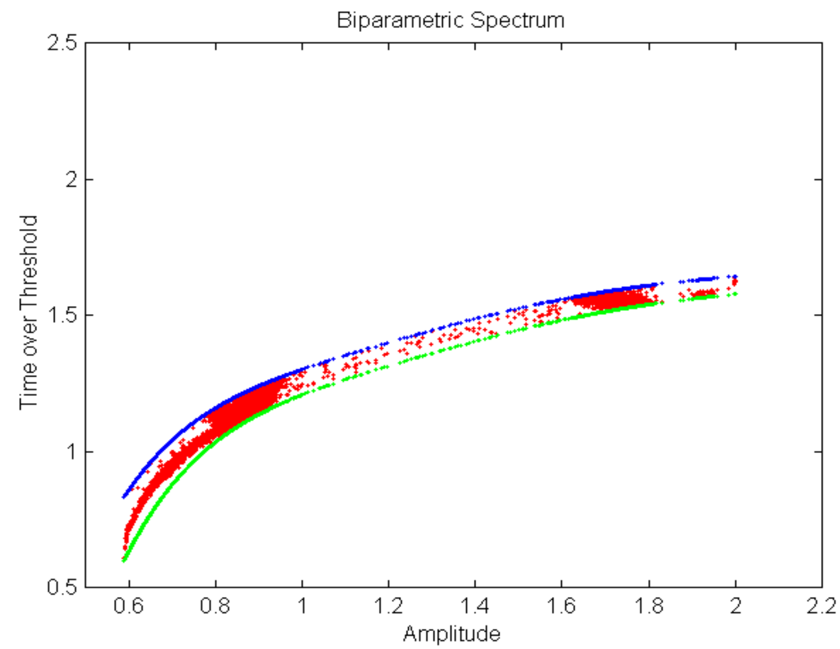


Time-Over-Threshold Measurement for pile-up rejection

The Pile-Up Rejection Algorithm

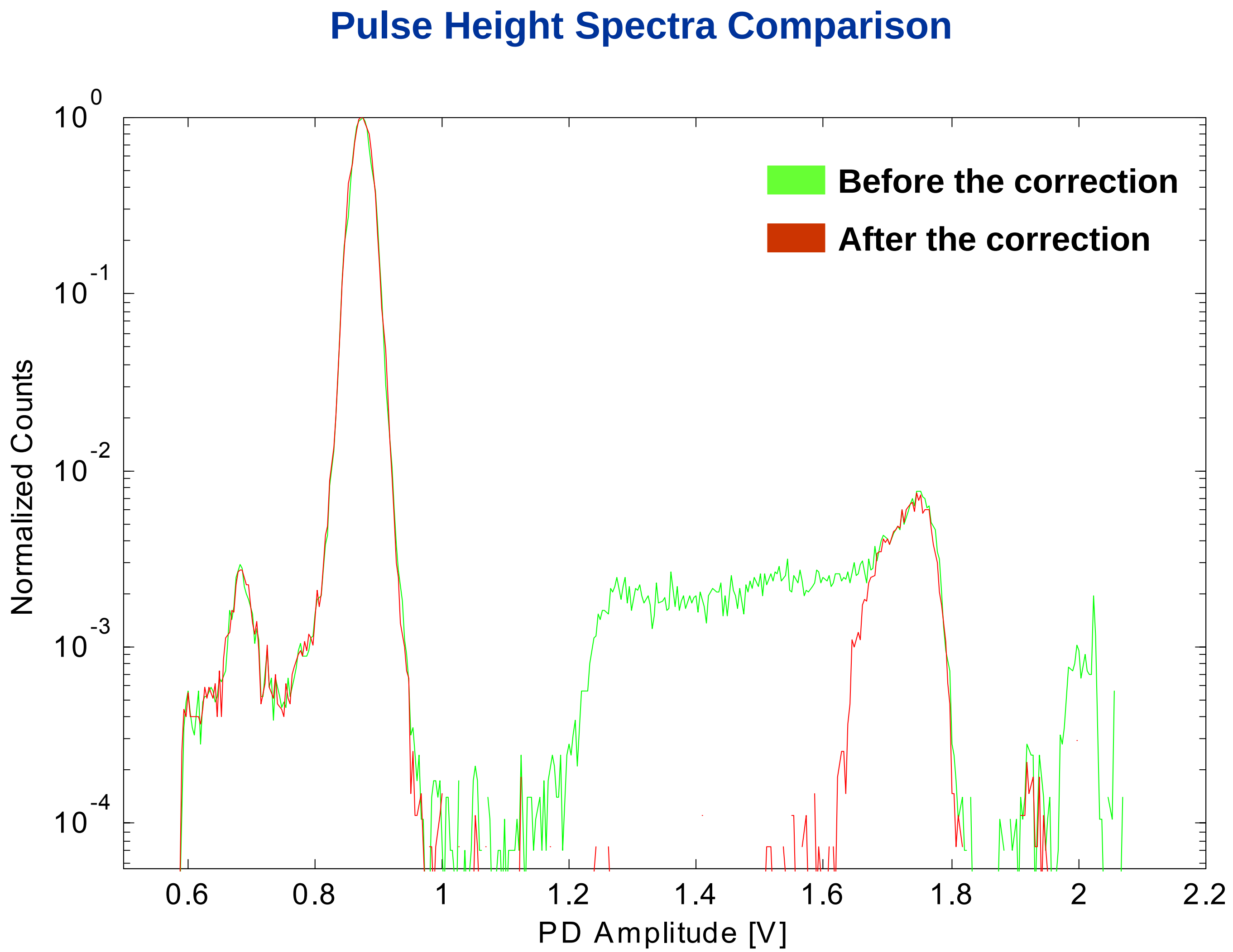


Before The Correction

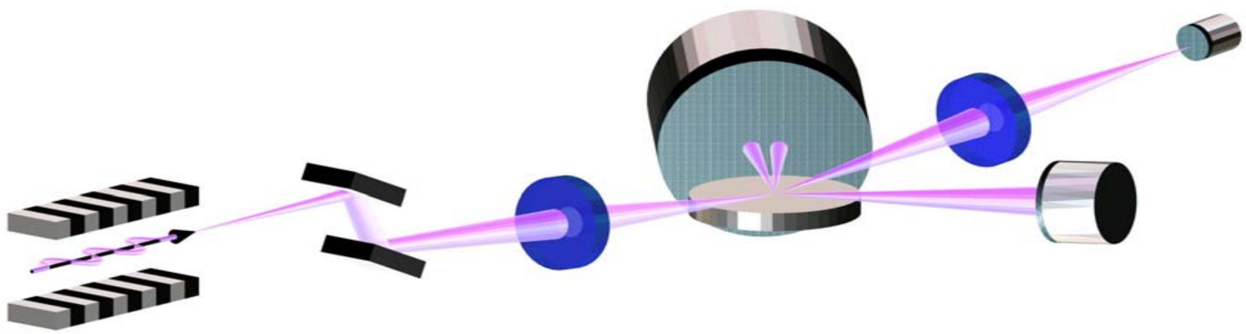


After The Correction

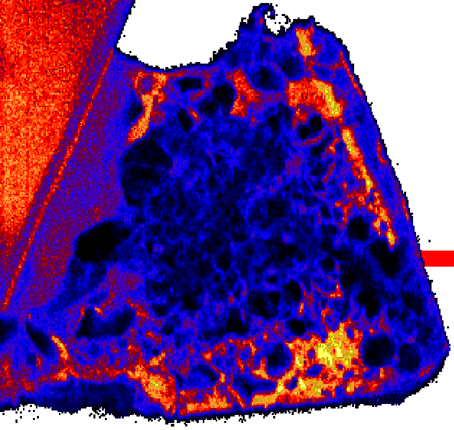
Time-Over-Threshold Measurement for pile-up rejection

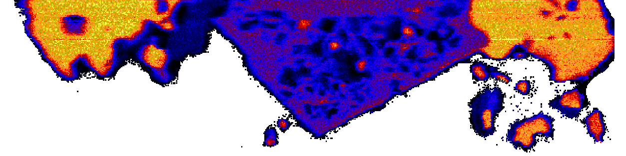


Generic microprobe schematic

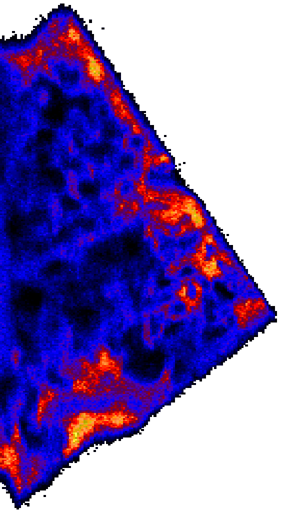


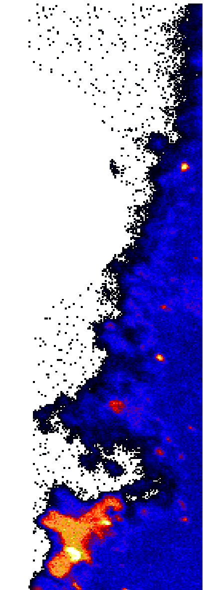
- Includes facilities for
  - fluorescence (multi-element detector)
  - diffraction (fast readout area detector)
  - microscopy (full-field ZP microscope)





Quantitative Image Projection and High Speed Detector Array for Real-time Synchrotron XRF Elemental Imaging using the X-ray Microprobe

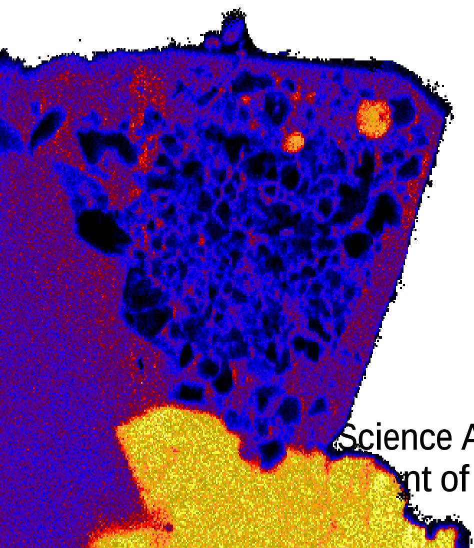


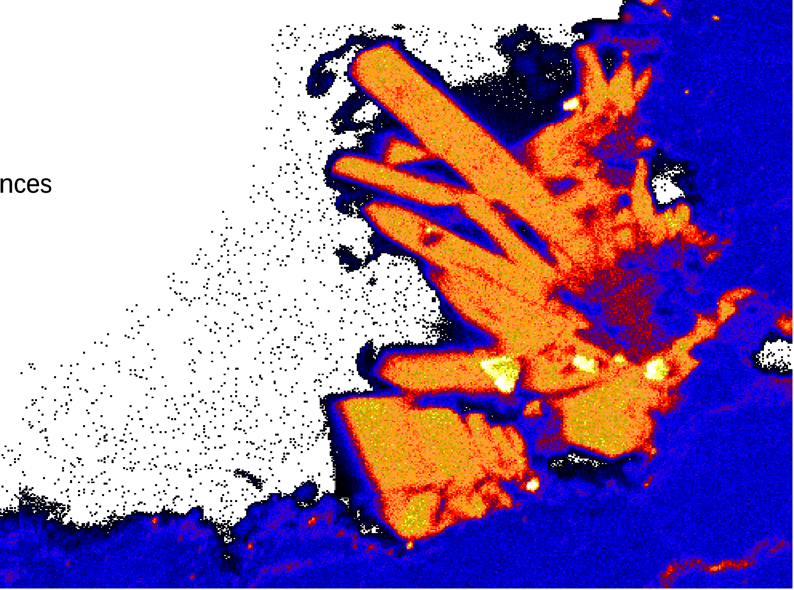


Chris Ryan[1,2], Peter Siddons[3], Angelo Dragone[3], Paul Dunn[4], Gareth Moorhead[4,2] and Barbara Etschmann[1,5]

[1] CSIRO Exploration and Mining, Clayton VIC, Australia
[2] Physics Department, University of Melbourne, Parkville VIC, Australia
[3] National Synchrotron Light Source, Brookhaven National Laboratory, Upton NY, USA
[4] CSIRO Manufacturing and Infrastructure Technology, Preston VIC, Australia
[5] South Australian Museum, Adelaide SA, Australia

Work supported by:
U.S. Department of Energy, Office of Basic Energy Sciences





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Real-time Elemental Imaging …

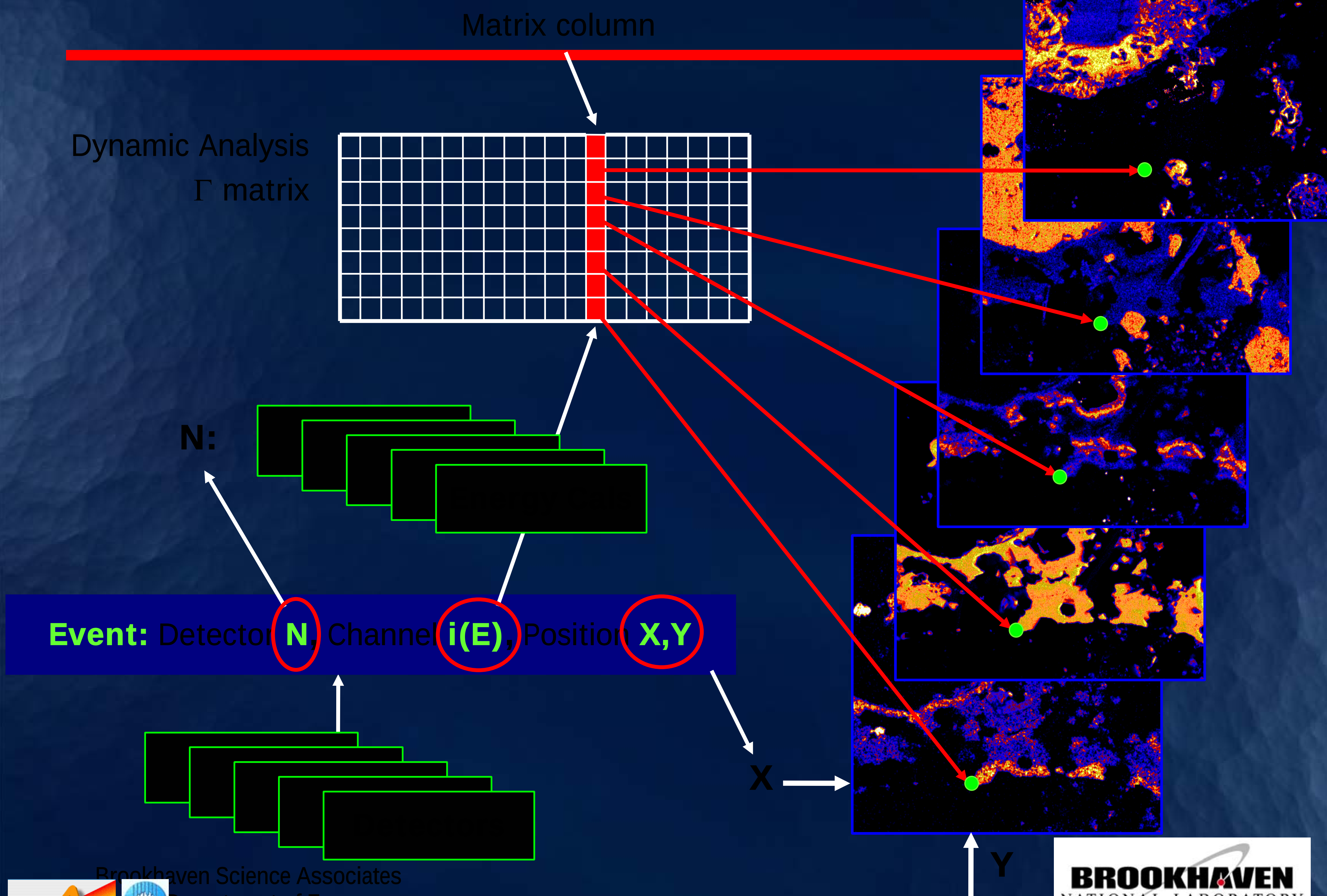
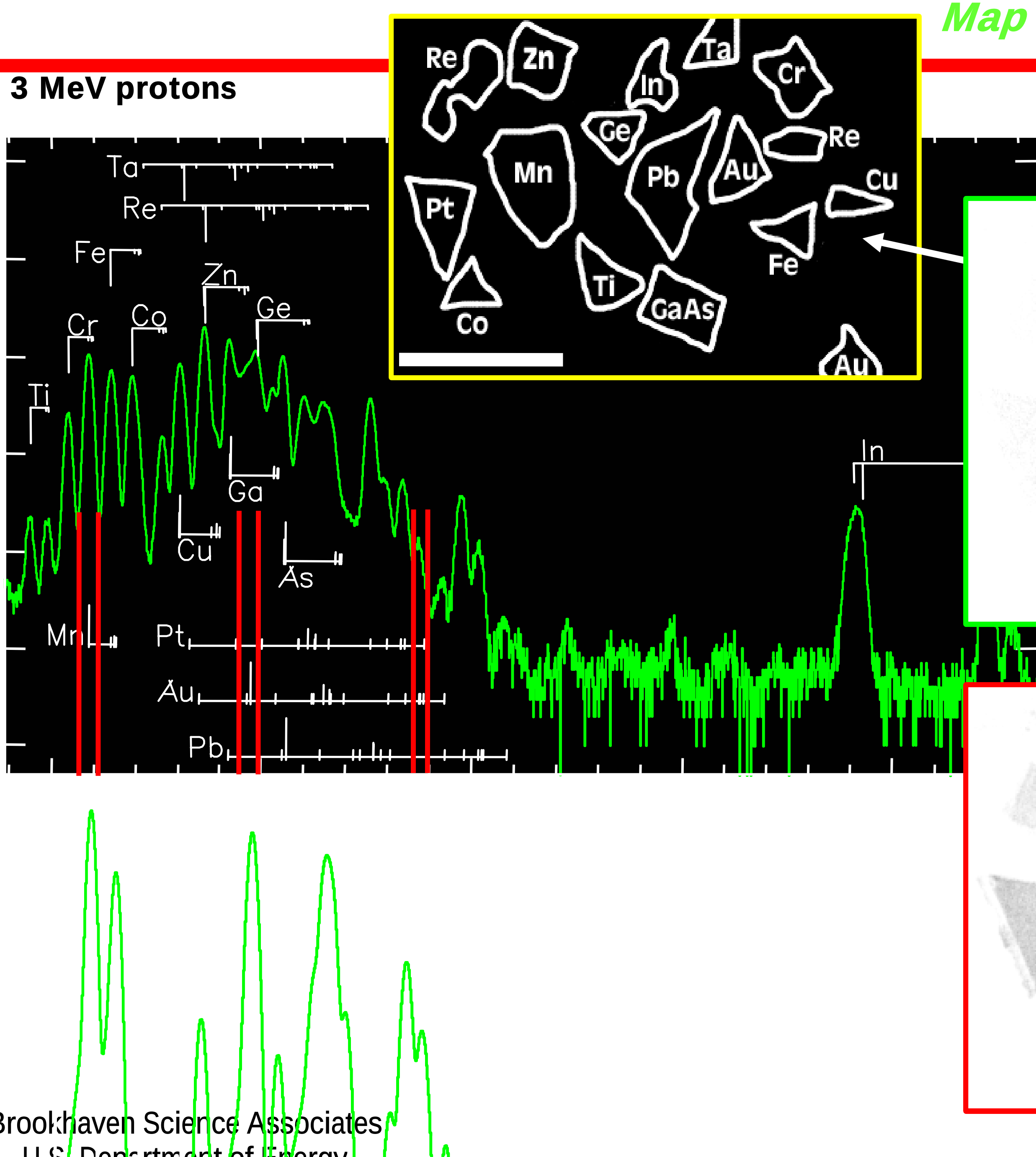
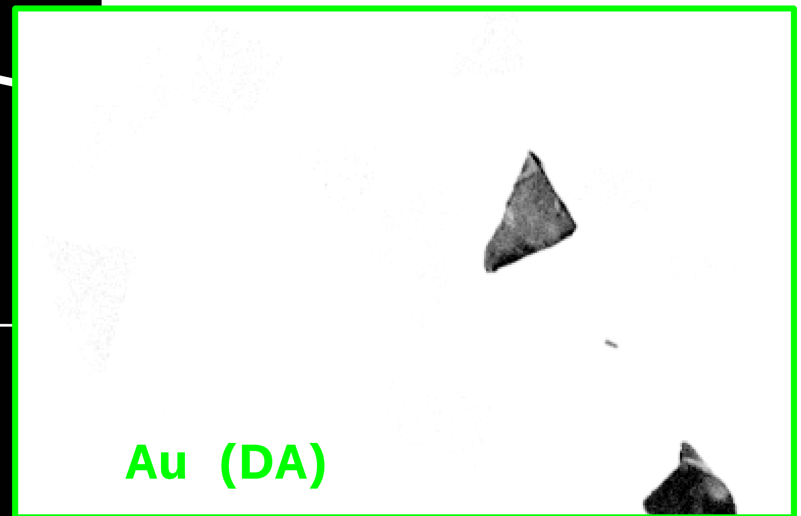


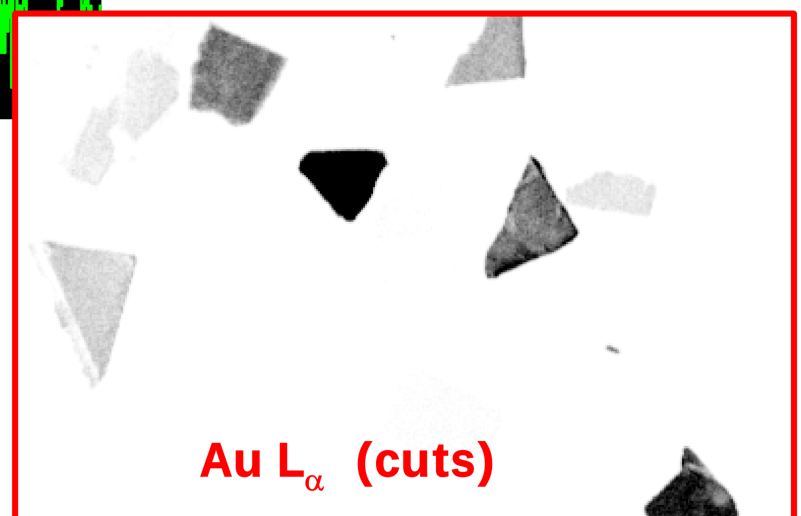
Illustration of Dynamic Analysis using PIXE

Map

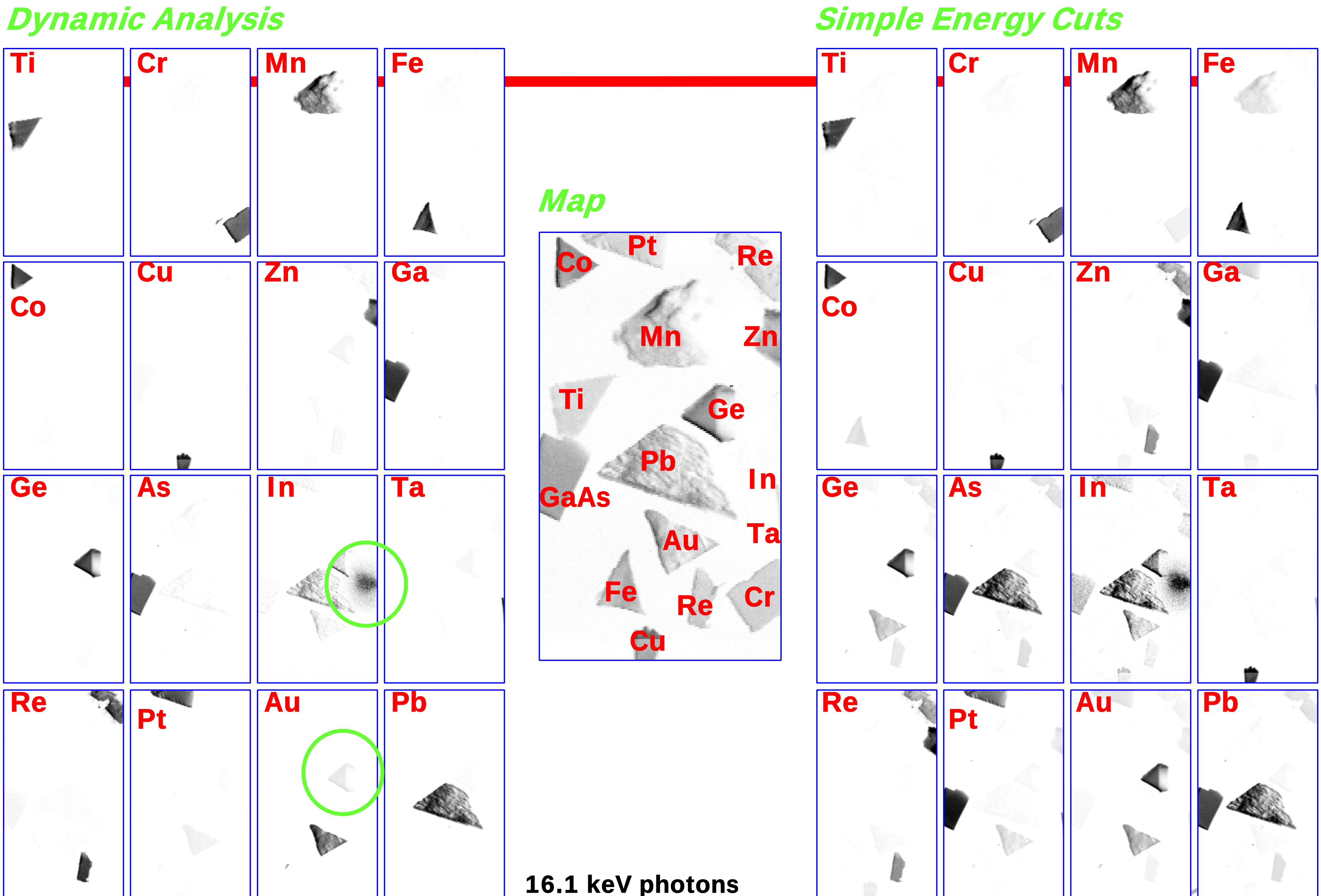
3 MeV protons





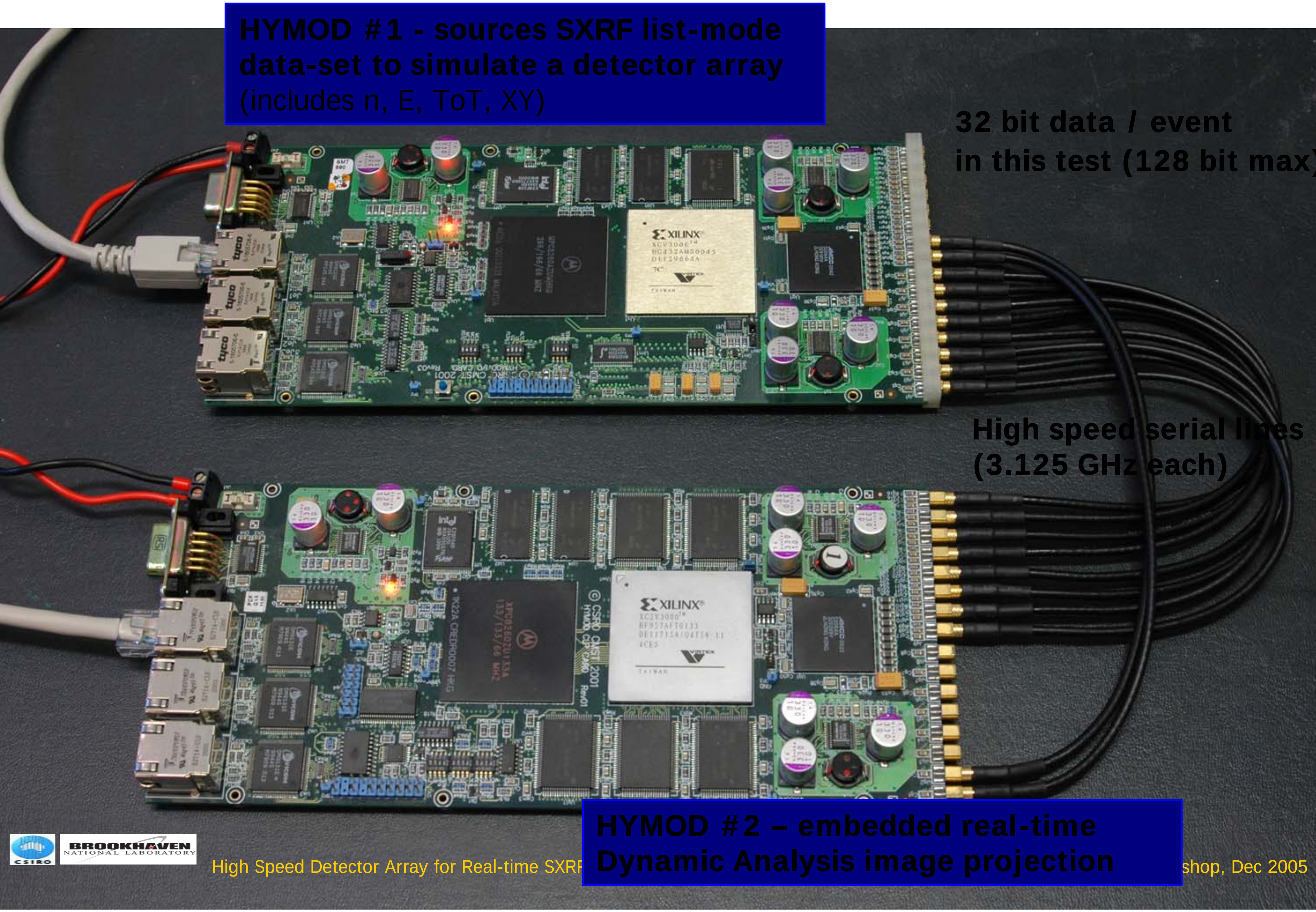


Test of Dynamic Analysis using SXRF



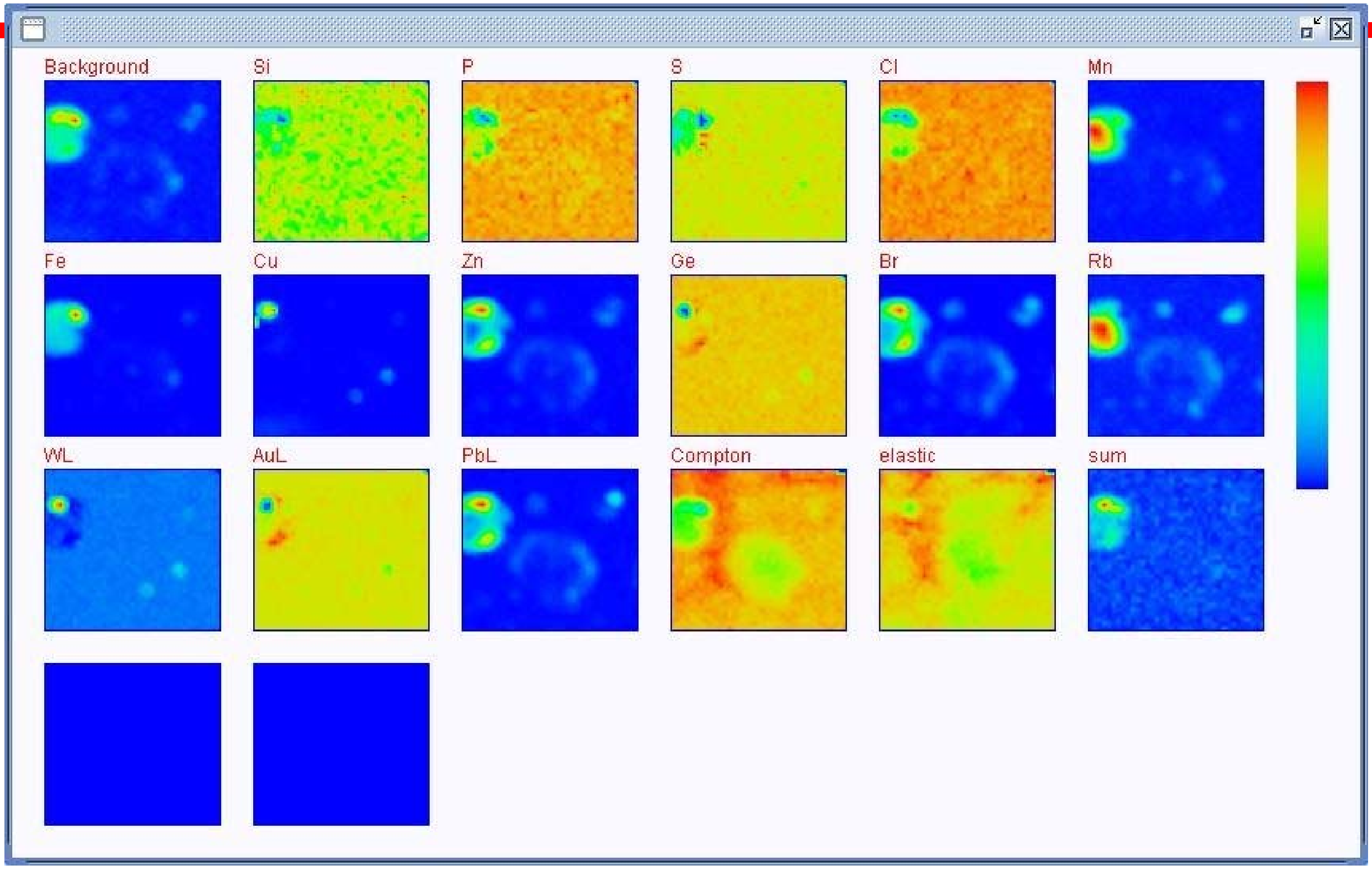
16.1 keV photons

Test of Real Time SXRF Imaging using Hymod



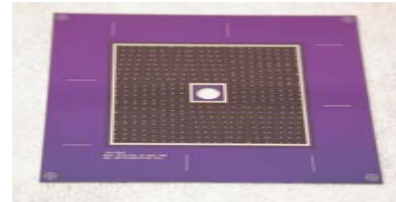
Test of Real Time SXRF Imaging using HYMOD

25 M events in test data-set (fluid inclusions; APS 2-ID-E; simulate ToT) ...



... processed in HYMOD #2 using Dynamic Analysis into elemental images in 250 ms, at 100 M events per second (400 Mbytes/s).

Conclusions



BNL 384 element Si detector array development:

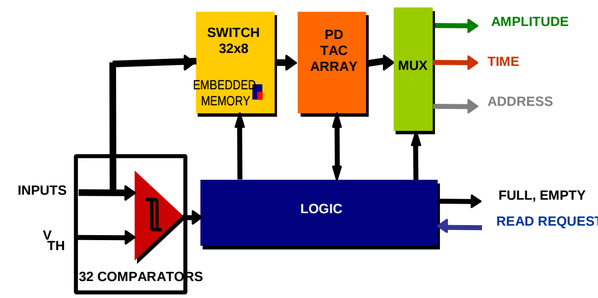
Pre-amp/pulse shaping demonstrated in Hermes ASIC.

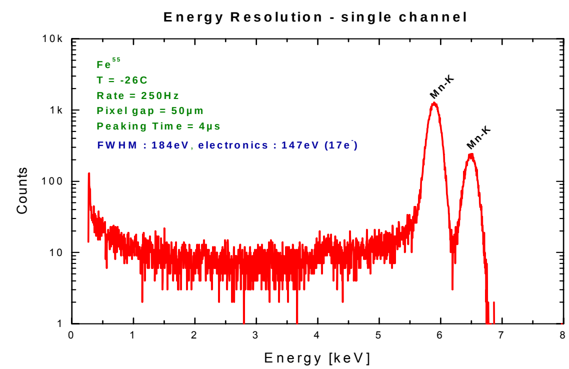
Achieves 184 eV resolution (Mn Kα).

New ASIC demonstrates peak-detecting de-randomizer, 32:1 multiplexer and ADC.

Time-over-threshold demonstrated for pile-up rejection.

Metal absorption mask demonstrated to control charge-sharing between detectors.





Real-time quantitative SXRF imaging:

Concept developed for real-time processing using CSIRO HYMOD pipelined, parallel processor.

De-coupling of data acquisition from stage control for fast scanning (XY sampled into data stream).

Dynamic Analysis method demonstrated for imaging of SXRF data off-line (APS sector 2; PNC-CAT, sector 20).

DA real-time deconvolution demonstrated at **10⁸ events/second** using HYMOD.

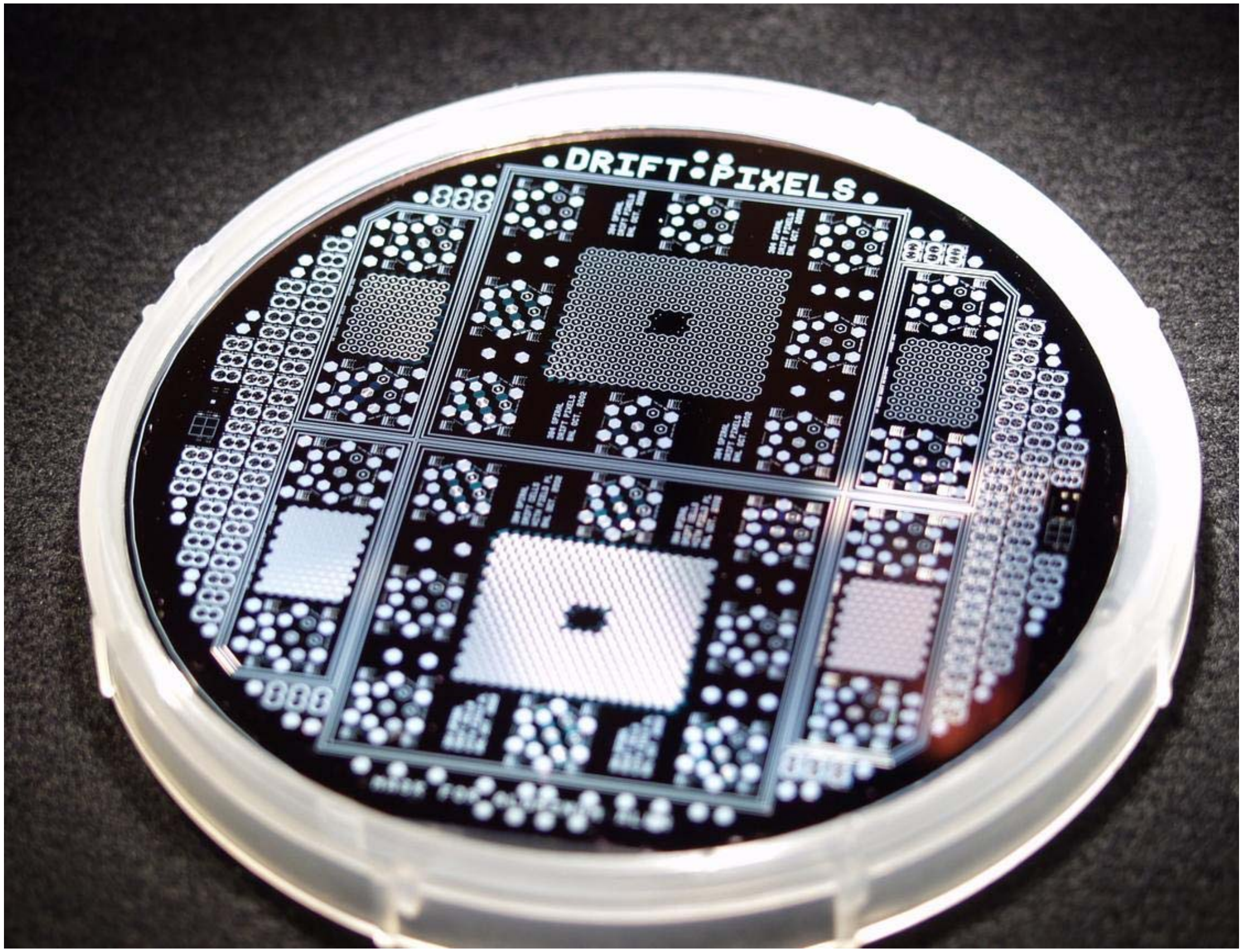
Drift-Detector Array (P. Rehak, W. Chen)

Drift-detectors give large area while keeping low capacitance by ‘drifting’ charge through bulk of silicon to a small collector electrode.

This device collects holes, to suit HERMES input stage.

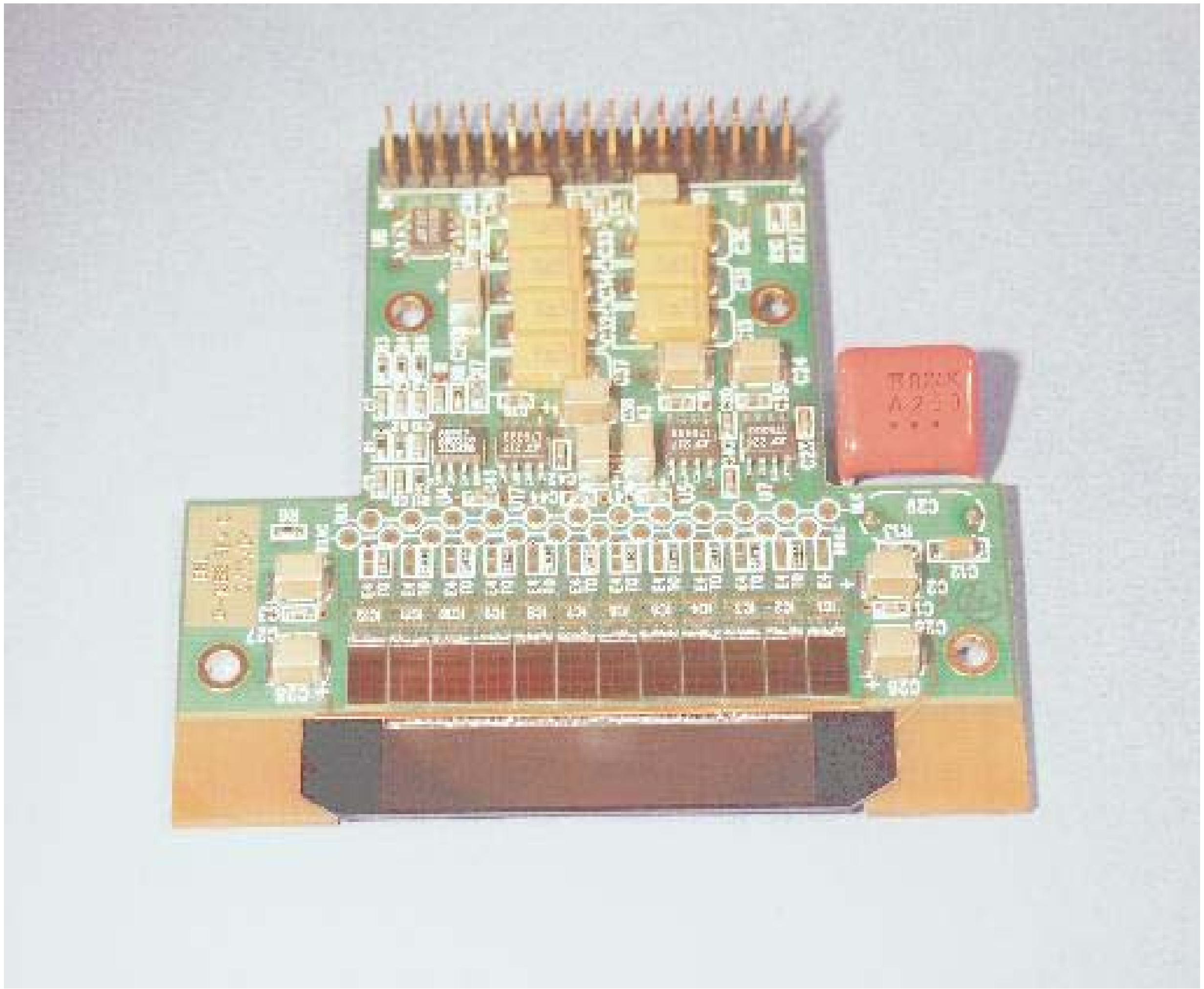
Wafer has 96- and 384-element arrays.

Not yet working :(



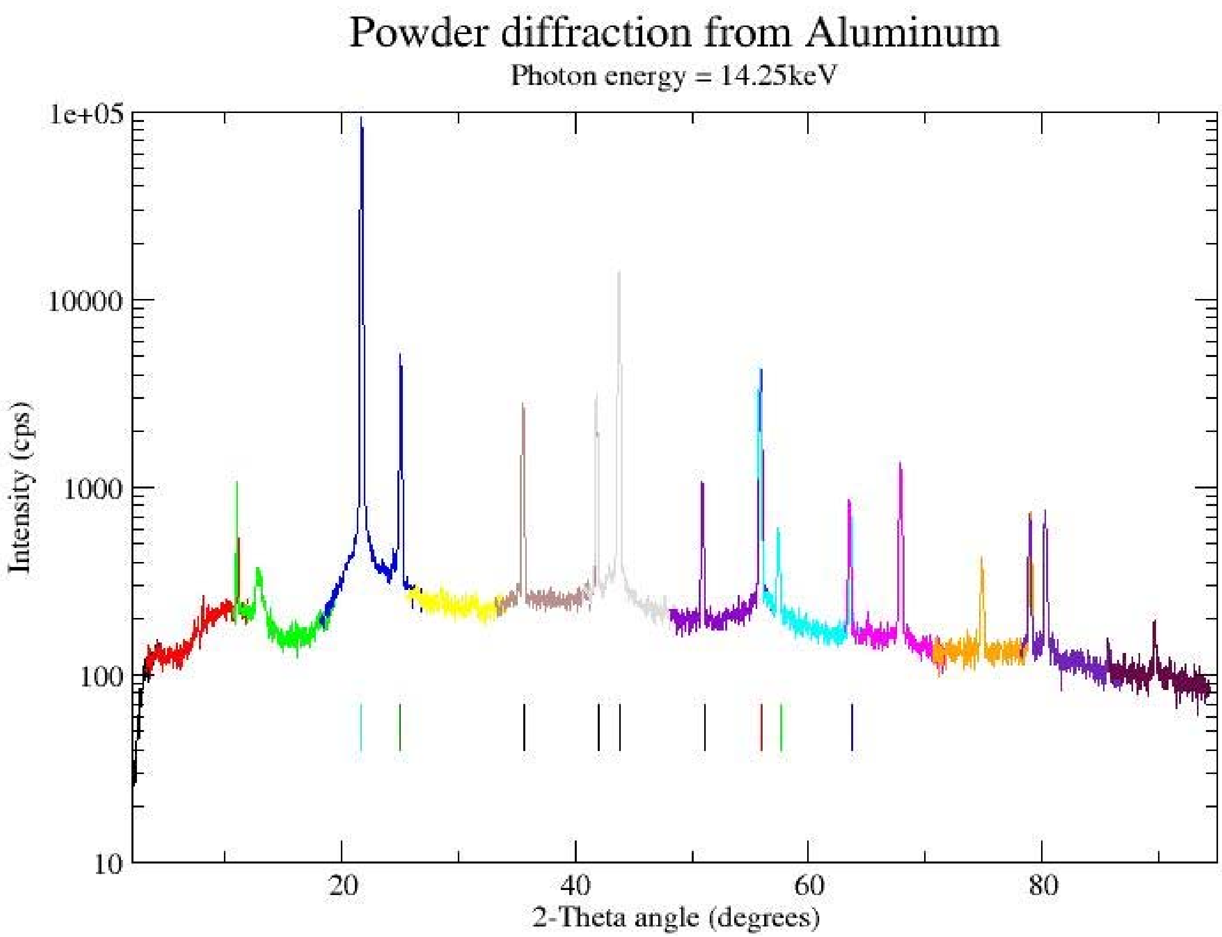
Diffraction / scattering applications of HERMES

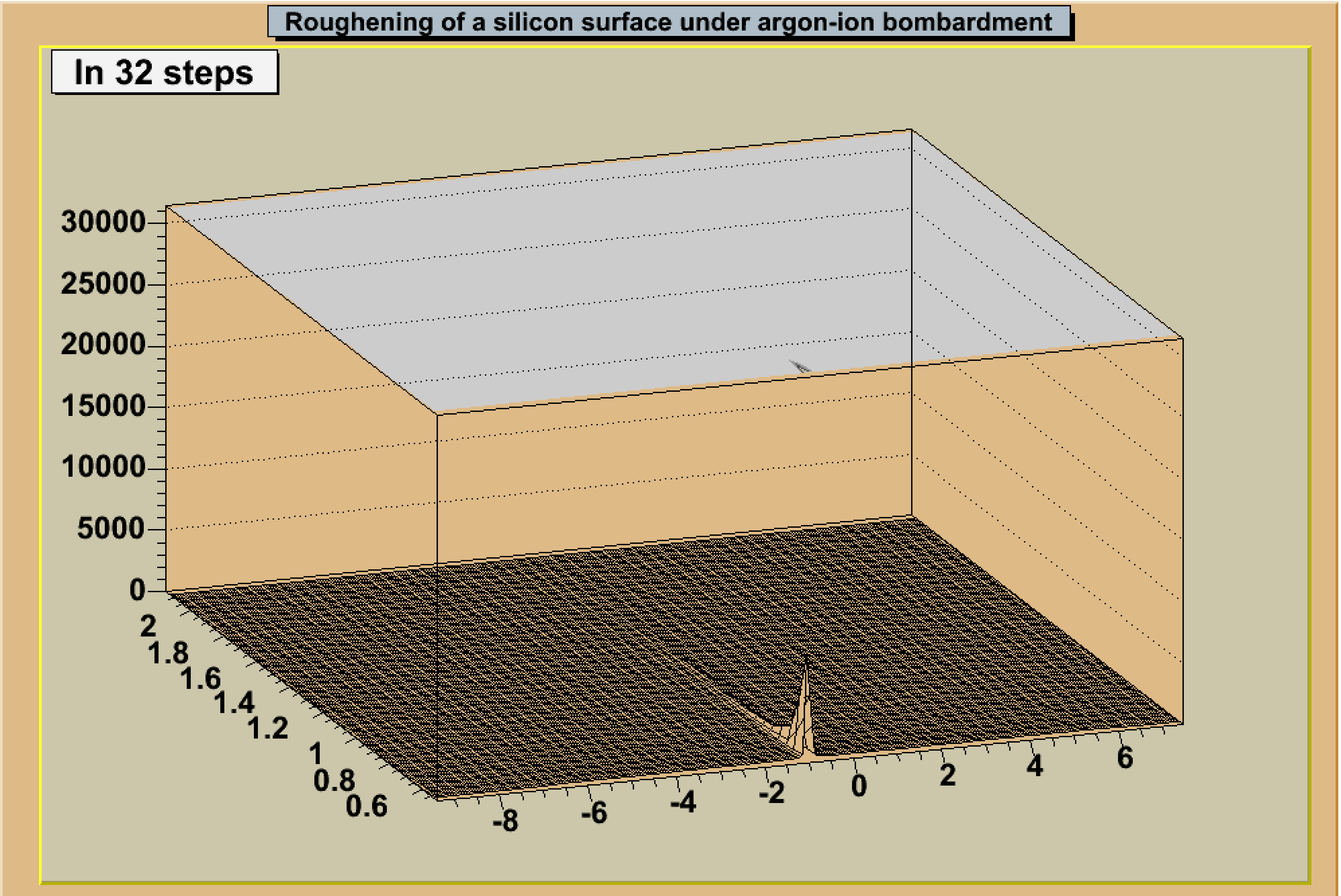
- Strip-shaped pixels form a 1-D position sensing detector with energy resolution (~350eV).
- 320 strips on 0.125mm pitch -> 40mm total length
- Strips 8mm long
- Useful for diffraction and scattering experiments.



Powder diffraction

- Detector length = 40mm
- Sample-detector distance = 263mm
- -> 8.7 degrees coverage 0.03 degrees / strip.
- 13 measurements spaced 7.5 degrees apart, each 1 second count time.
- Total 20 sec. scan.



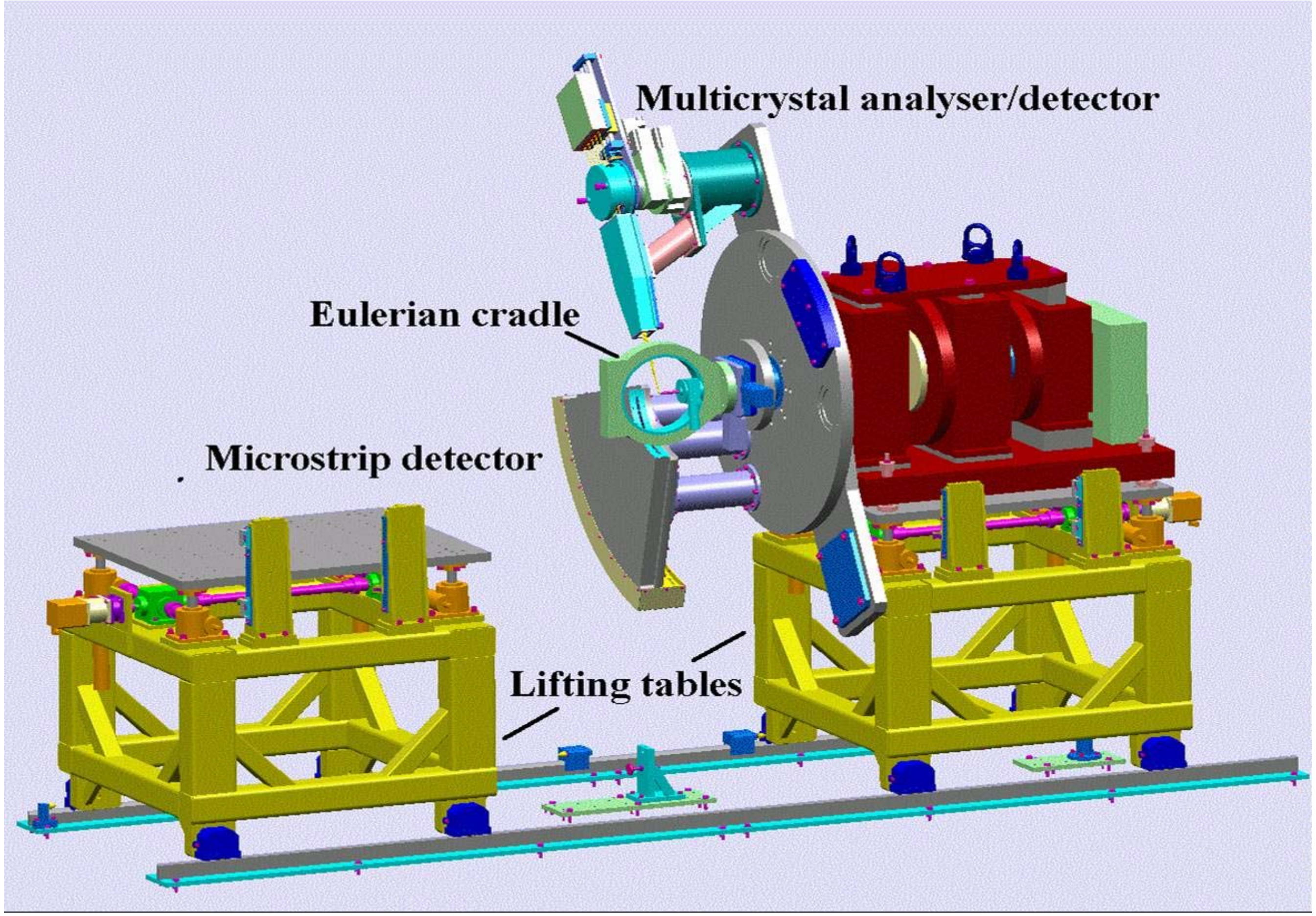

Roughening of a silicon surface under argon-ion bombardment
In 32 steps
30000
25000
20000
15000
10000
5000
0
2
1.8
1.6
1.4
1.2
1
0.8
0.6
-8
-6
-4
-2
0
2
4
6

Next steps

- Use existing HERMES technology to make full-coverage powder camera (collaboration with Diamond)
  - ~10,000 strips
  - Fast FPGA-based readout, <1ms.
- Make optimized version of HERMES for diffraction / scattering applications.

SLS powder diffractometer

- Uses MYTHEN strip detector plus crystal array
- Diamond instrument will use HERMES initially, and an optimized version or a new custom design as an upgrade.



Pixel structure of XAMPS detector for LCLS

- Low-resistivity layer is formed by deep implant.
- JFET switches are fabricated in this layer
- Charge is produced by photoionization
- Electrons collect under pixel (switch is OFF)
- Charge is read out by turning transistor ON, connecting stored charge to a buss-bar, and read out by a charge-sensitive amplifier.

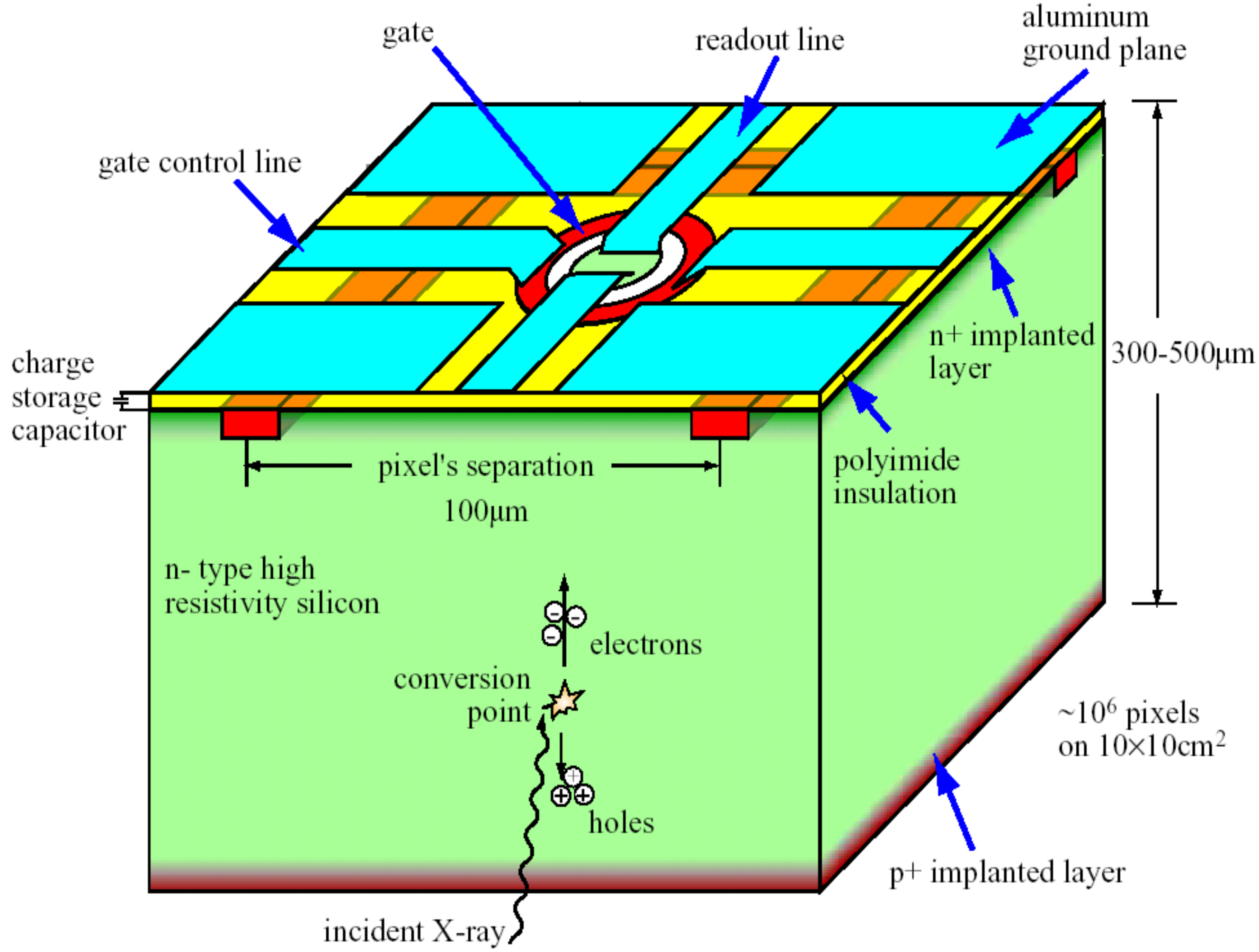
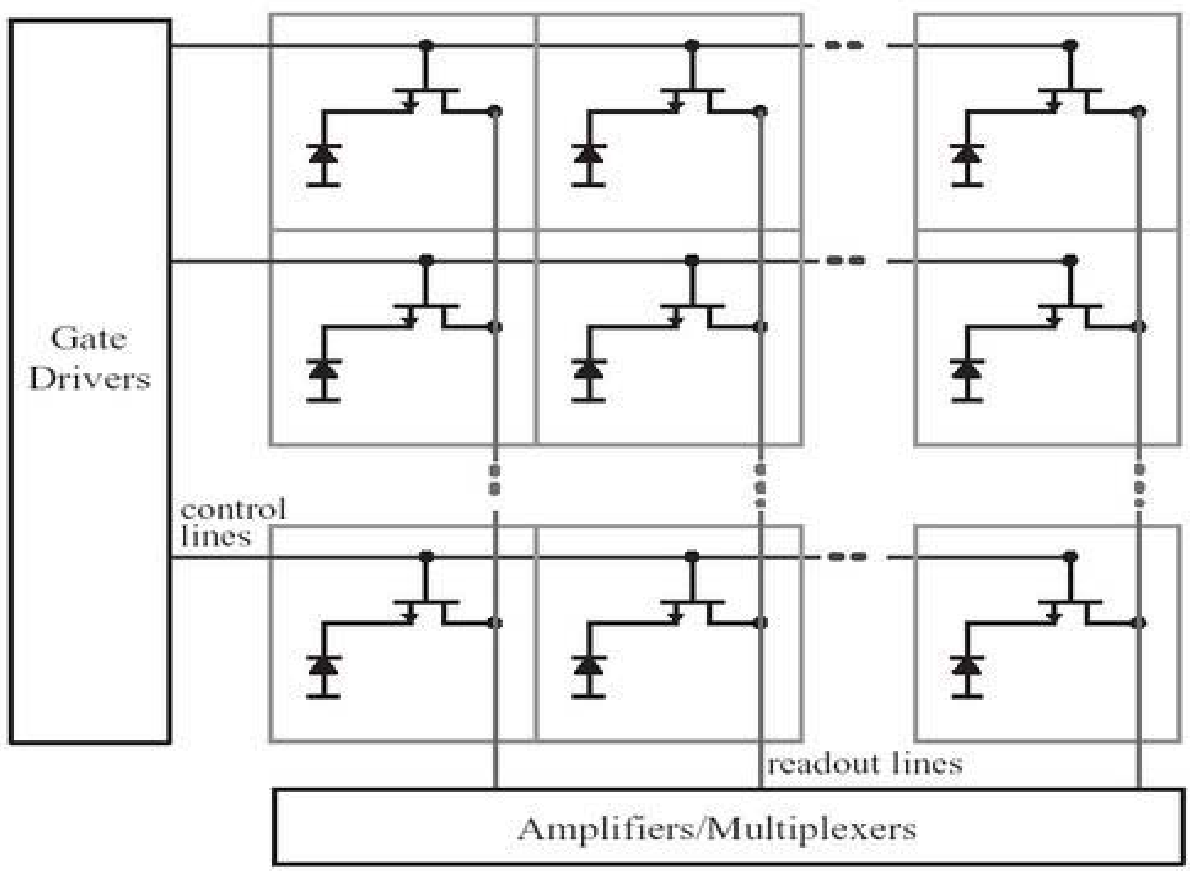


Figure 6. One pixel from an Active Matrix Pixel detector array. The device is fabricated by forming a low-resistivity silicon layer suitable for JFET switching devices on top of high-resistivity silicon optimized for detector fabrication. The JFET transistors formed in this layer are used to row-sequentially switch the collected charge into column output amplifiers.

Active matrix readout

- Charge stored in diode capacitance (switches off)
- Readout amplifier/ADC on each column
- Switches turned on sequentially row-by-row
- Charge read out and digitized
- 1us per row => 1ms for 1000 rows.
  - 8-channel 40MHz/channel ADC chip exists
  - 32 chips, each ADC multiplexed among 4 columns
  - 2Gb/s data rate



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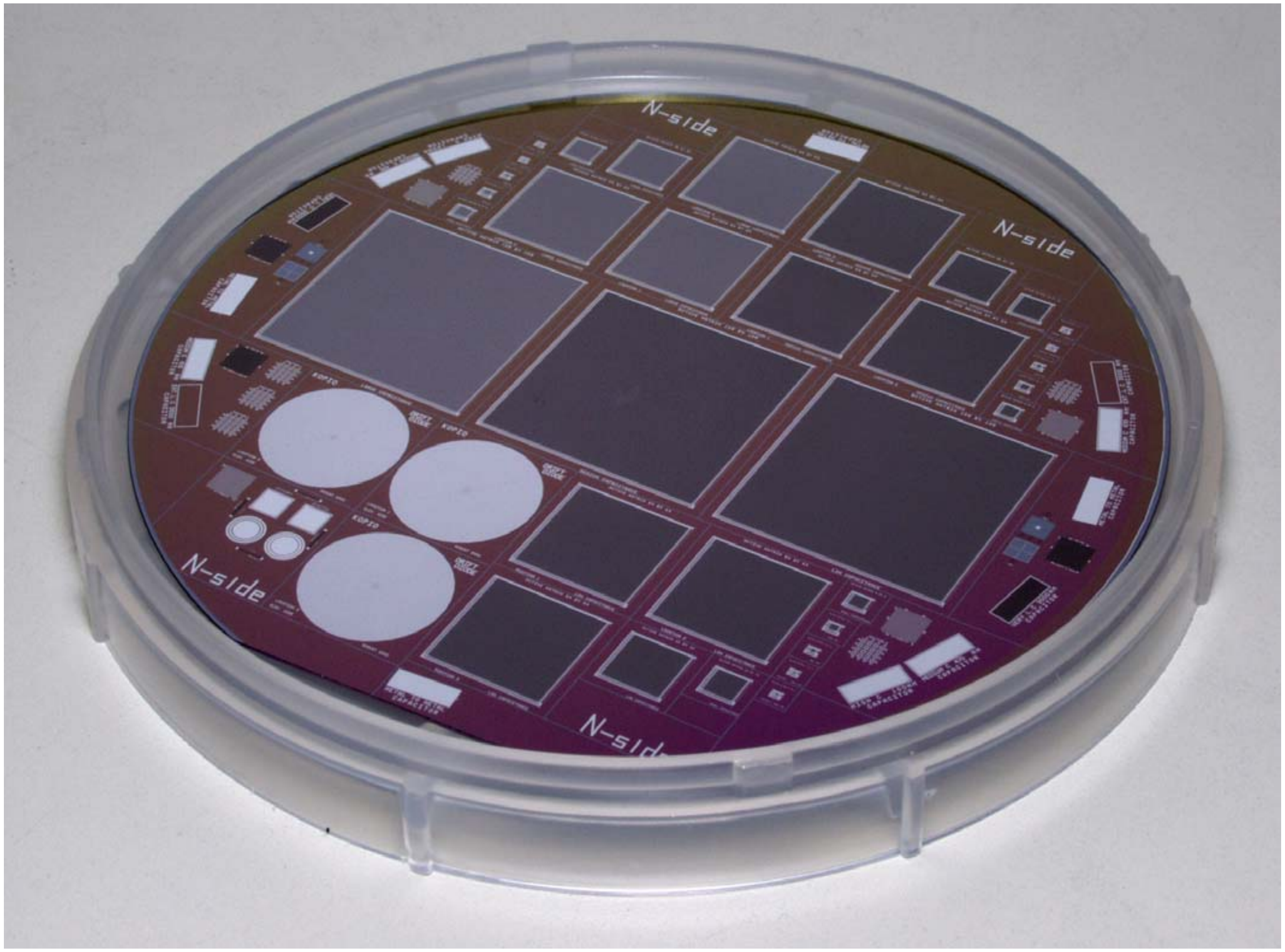
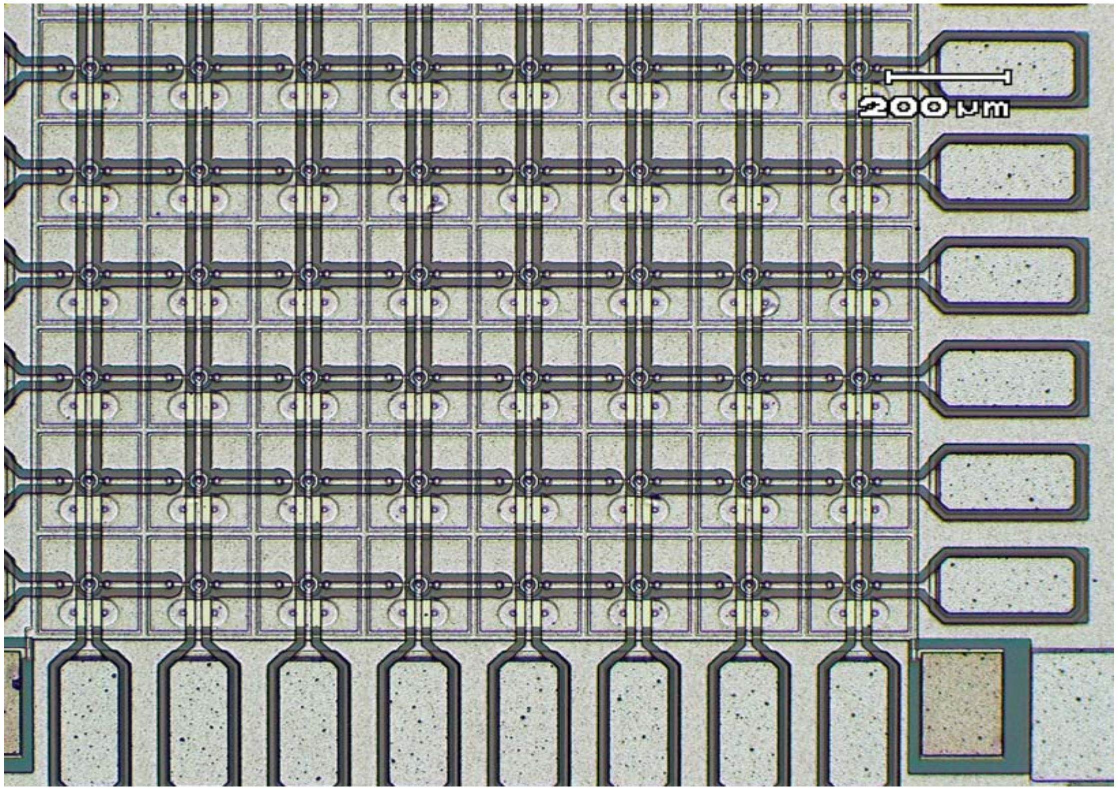
View of a completed wafer



Prototype device

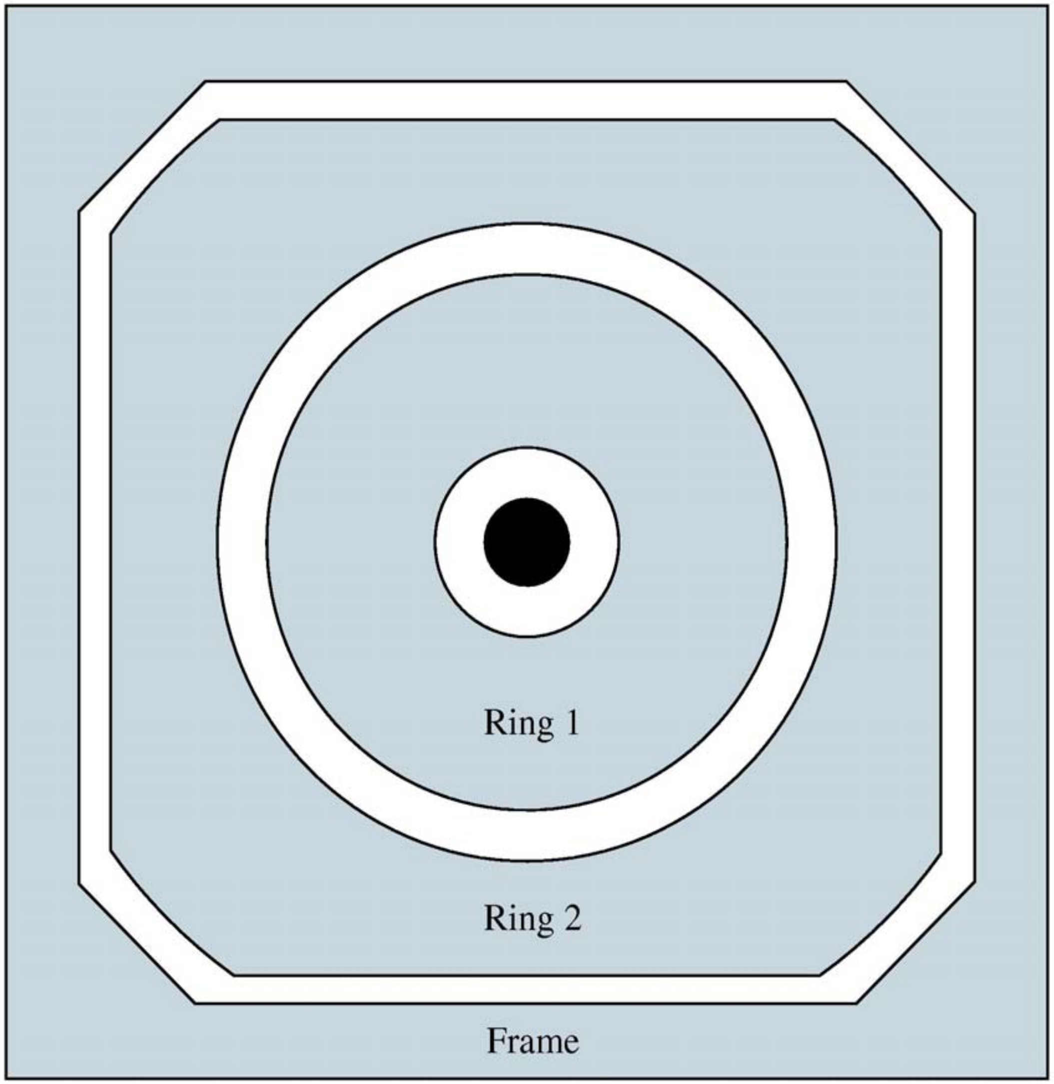
- Part of an 8 x 8 pixel test device
- 180 um square pixels



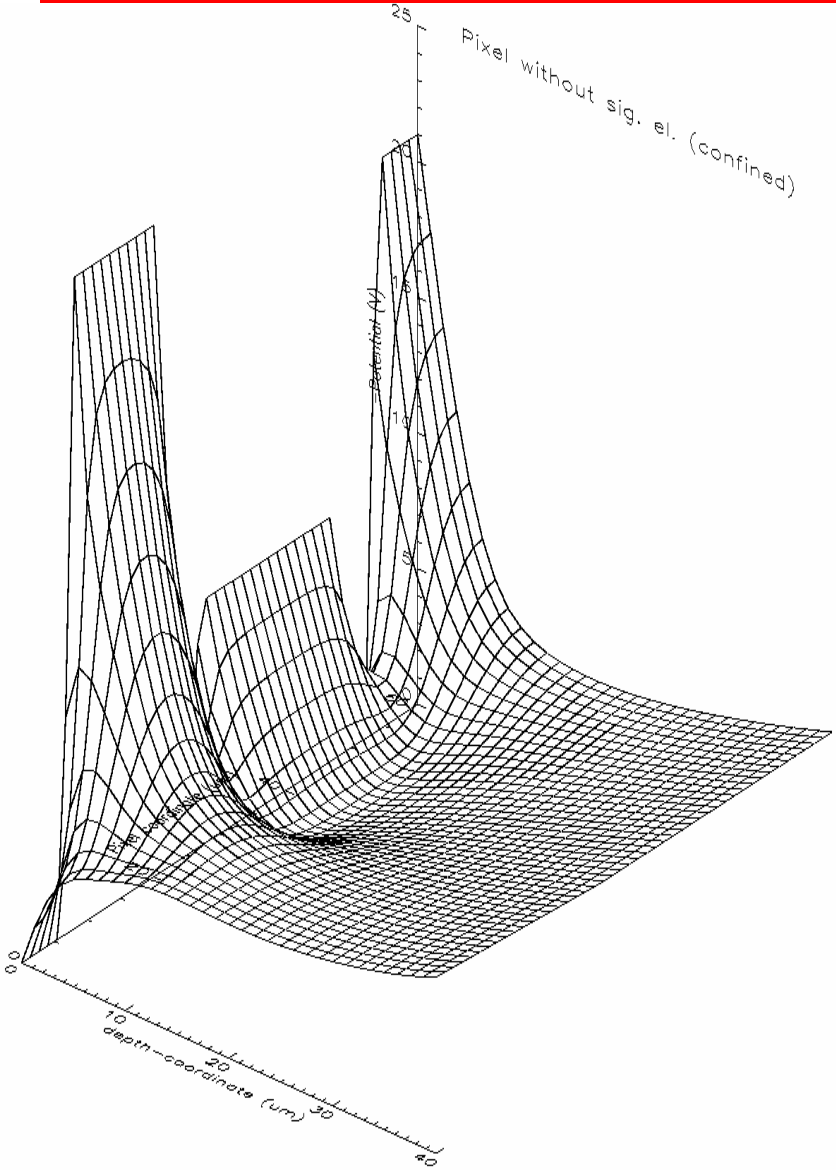
Alternative small-pixel structure

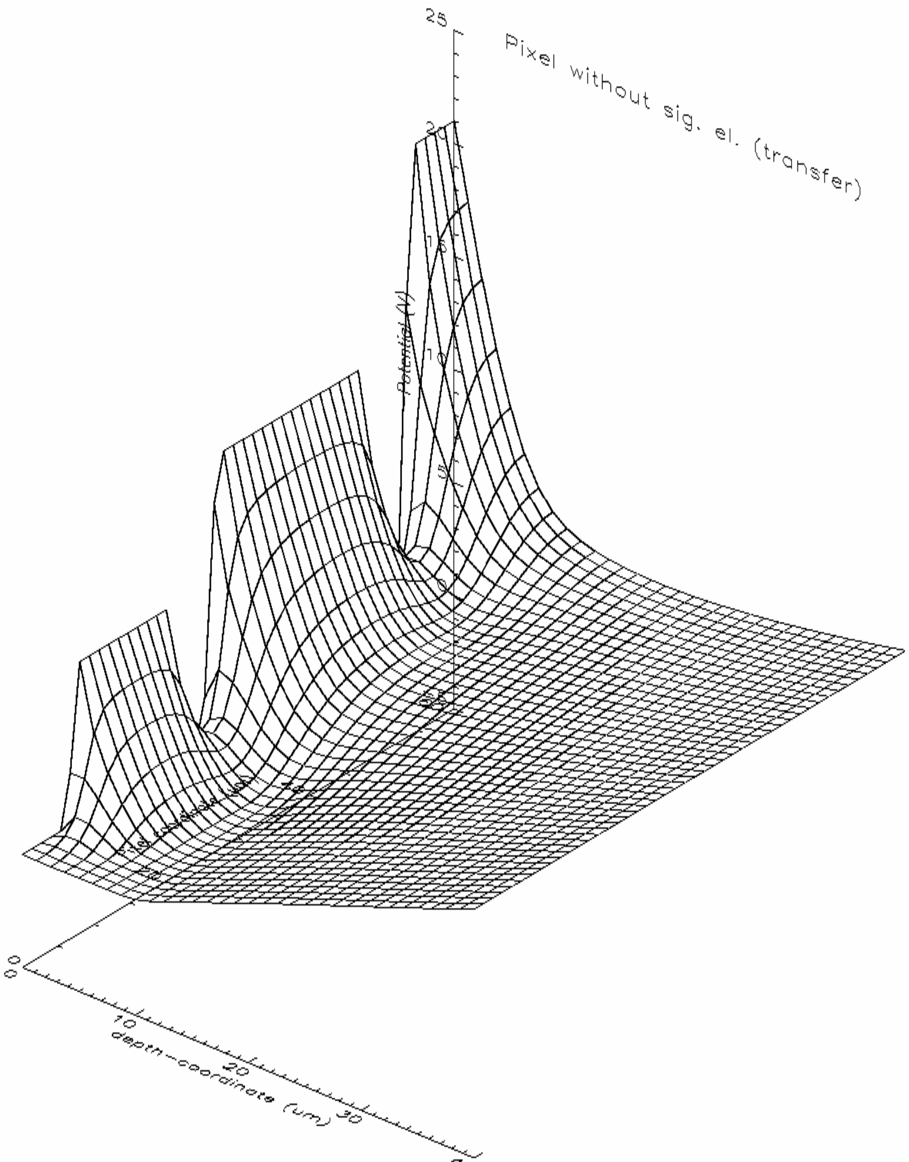
- Small pixels are difficult with transistor switch
- Charge can be stored in potential well and released in a controlled way, similar to drift detectors.
- This 'charge pump' technology is ideal for speckle applications.

Top view of a pixel with a charge pump single transfer



Charge pumping (no transistor)





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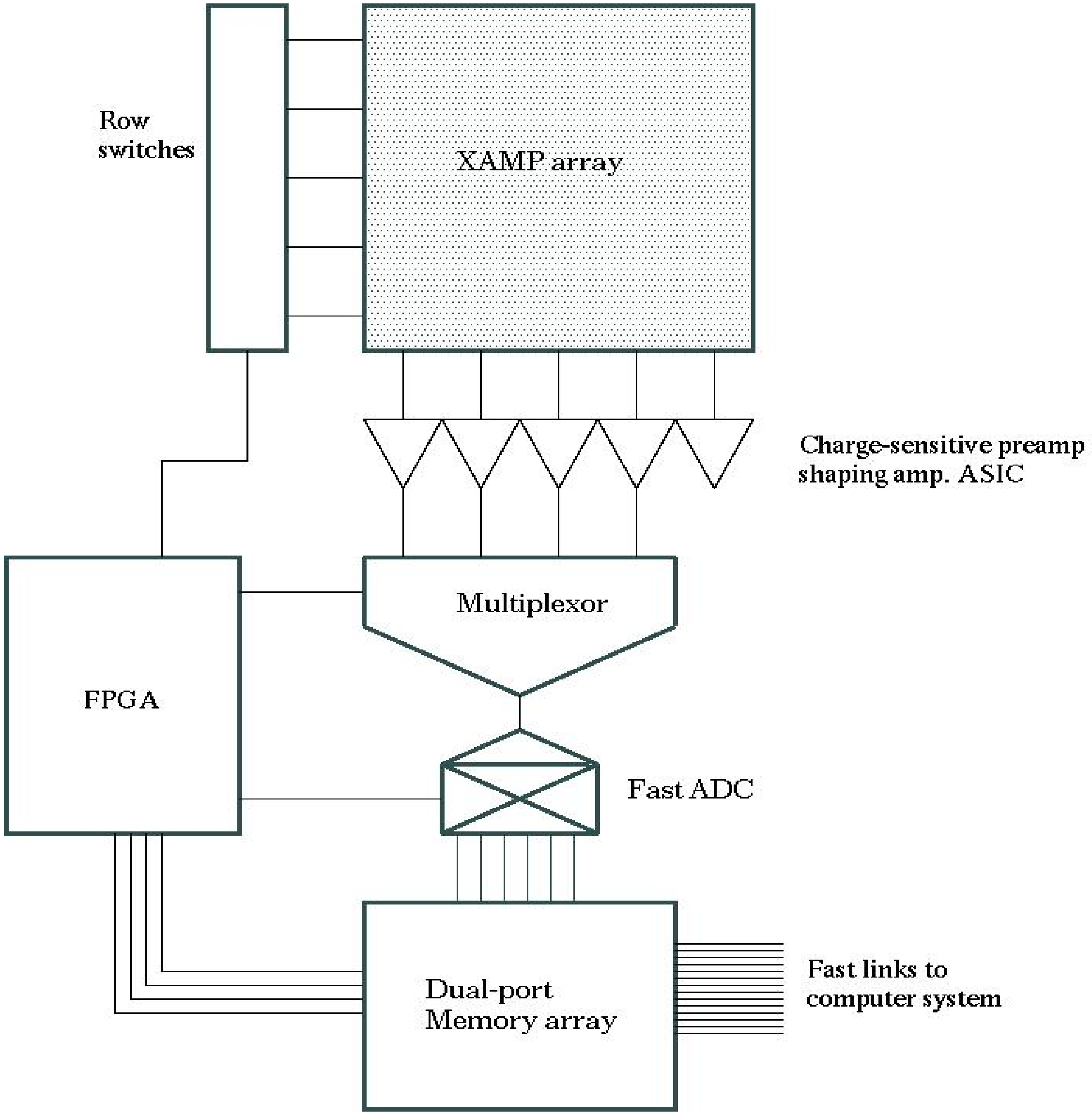
Readout system

- Row-by-row readout, 1us/row
- 32 Fast (>20MHz) 8-channel ADC's multiplexed e.g. x4 = 1024
- 2Gb/s
- Data streamed through FPGA to fast memory and terabyte disk store.



Summary

- We have developed an ASIC for low-noise photon-counting applications, and combined it with low-leakage silicon diode-based detector elements; square pads for spectroscopy and strips for diffraction.
- We are applying these detectors to problems in X-ray spectroscopy, scattering and diffraction
- They provide low noise (good energy resolution) and high count rate.
- We have made progress on a next-generation spectroscopy chip set and advanced pulse processing for microprobe applications.
- We are working with LCLS to provide area detectors.
- We have collaborations with other institutions to leverage these developments to provide practical systems for beamlines.