The IPNS Data Acquisition System

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Introduction

The Intense Pulsed Neutron Source at Argonne National Laboratory is in the process of upgrading the data acquisition system [1][2][3][4] used on its neutron scattering instruments. The current system uses a combination of CAMAC and Multibus hardware together with a VAX computer linked to the system with a Q-Bus/Multibus interface. This hardware is being replaced primarily due to age. Over time we have been experiencing problems with module reliability and procurement (due to obsolescence), as well as system speed and flexibility.

The new system was designed with goals to provide higher reliability, higher system speed and better diagnostics; to be built on modern components and allow for a user interface that is independent of the choice of user computer. The system chosen consists of custom VXI modules for processing detector input and a commercial VME crate controller. A flexible network-based connection based on the Experimental Physics and Industrial Control System (EPICS) [5][6] is provided between the user interface computer and VXI mainframes.

System Overview

The backbone of this data acquisition system is the VXI mainframe. Each mainframe will be equipped with one I/O controller (IOC), one Readout Control (ROC) module and up to eleven Time-of-Flight Histogramming (TOF) modules. Each of the neutron scattering instruments will have one or more of these VXI mainframes and one or more user interface computers (Fig. 1). The number of detectors in the instrument will determine the number of mainframes. For our single element detectors, each module is designed to handle the input from sixteen detectors. The first instrument to be converted to this new system will be the High Resolution Medium Energy Chopper Spectrometer (HRMECS) which has approximately 420 detectors. This instrument will therefore require a minimum of 3 VXI mainframes holding 27 TOF modules.

VXI mainframes will be connected to each other and to instrument control/user interface computers using the Ethernet adapter on the IOC. Communication between the IOCs is done using TCP/UDP protocols (i.e. NFS, FTP, Telnet and EPICS Channel Access).

The primary means for control of the system is EPICS based software. EPICS allows hardware parameters to be linked to network-accessible "database" records. Each record (e.g. a detector's discriminator level) in this database is assigned a unique name and is made available via the EPICS Channel Access server that runs on the IOC.

Module Descriptions

TOF Histogramming Module

The TOF histogramming module is a custom VXI module (Fig. 2). This module was designed to allow flexibility on the detector-input side of the module. Detector inputs are first routed through one of eight changeable personality modules (based on the common 72 pin SIMM form factor) whose output is processed by that channel's Field Programmable Gate Array (FPGA). The main system board was designed to accommodate either sixteen single element detectors or eight double-ended position sensitive detectors (PSD) by changing the SIMM module and the corresponding FPGA code. This paper will describe work done with single element tubes with PSD plans treated with future plans.

A block diagram of the TOF module is shown in Figure 3 and the single element SIMM is shown in Figure 4. Detector input from a differential amplifier is brought onto the main board via two of the pins on a front panel DB-37 connector (16 detectors x 2 pins uses 32 of these pins). This signal is routed to one of the eight SIMM modules. The FPGA for a channel starts a 20-bit time counter that is driven by a global 10MHz clock at the start of each accelerator pulse (T_0). When a neutron event occurs it is time gated,

buffered and then compared to a lower level discriminator (LLD) on the SIMM module. The LLD comes from a 12-bit DAC on the main board. When the signal level goes above the LLD, an event trigger is raised which goes to the FPGA for that detector. The FPGA then latches the 20-bit time counter. The FPGA converts the latched time to a 16-bit number using a RAM lookup table. While the time conversion is in progress, the SIMM module performs an 8-bit ADC on the peak voltage. This number is serially transferred to the FPGA where a digital compare is performed against an upper level threshold. If the event is above that threshold, it is vetoed locally. If the event is below the threshold, the module's readout control (MRC) FPGA is notified that the channel has data. The MRC FPGA moves the data into a FIFO Ping-Pong frame buffer where it is stored until the next T_0 pulse. When the next accelerator pulse occurs the MRCFPGA switches to the other FIFO in the Ping-Pong buffer and allows the IOC to read the data from the last T_0 frame from the original buffer.

Data passed to the FIFO is in the form of a 32-bit word. The lower 16-bits of this word is a histogram offset and the upper 16 bits is a block offset. The block offset determines which histogram is to be incremented for this detector and is a parameter loaded into each detector's FPGA. The histogram offset determines an address within a particular histogram to increment and comes from the time conversion lookup table. Using this scheme, a number of detectors can be binned in the same histogram to conserve physical memory. Each of these detectors can also have a separate time lookup table so that detectors which are at different distances and angles can be time focused with the precision of the system clock (100nSec).

Readout Control (ROC) Module

The ROC module is designed mainly to provide some housekeeping tasks not performed by the other modules. The main function of this module is the collection of external control signals to be distributed on the VXI bus for use on the TOF modules. Signals input on the front panel include the accelerator pulse (T_0), system veto, three test input signals, and token input/output signals. This module also provides outputs from the Ethernet and serial lines of the IOC.

The T_0 pulse is an input to a front panel LEMO and is distributed to other modules on the VXI local bus. This pulse causes a hardware interrupt to the IOC which launches a routine to retrieve the data collected on the TOF modules during the previous T_0 frame.

The system veto provides a mechanism that prevents data collection during any T_0 frame. A pulse on this line during any frame resets the TOF module's readout control FPGA.

The test signals provide three unique signals that can be input via the ROC front panel and selectively passed along as an alternate detector input for diagnostic purposes. Note that it is also possible to provide software driven signals to the detector input.

The token input/output provides for an alternate multi-crate operation that will not be described here.

This module also generates a token that is passed to the first TOF module, via the VXI bus, to enable it to start placing its data on the VXI data bus for collection by the interrupt routine. After a TOF finishes placing its data on the bus the token is passed to the next module until all modules have dumped their data. When the last module places its data on the bus it returns the token back to the ROC and data processing is stopped for that T_0 frame.

Input/Output Controller(IOC)

The IOC is a commercial processor board. At present we are using a Motorola MVME167 board which is based on the 68040 processor and is available in 25 and 33MHz configurations. This processor board runs the VxWorks real-time operating system and EPICS software. The IOC is booted from a file server on the network and loads VxWorks, EPICS base software and some custom software for controlling our modules. EPICS provides means of network based control for data collection and a mechanism for tying together device drivers for the boards and the user interface. Device drivers are written and tied to "database" records on the IOC for a given function of the board. Input voltage discriminator levels, for example, are

tied to an analog output record, given a unique name and become accessible to the world via any computer that can communicate with an EPICS database using the Channel Access library.

As stated above, an interrupt service routine is linked to the T_0 signal on the ROC and initiates gathering data from the TOF modules. When this interrupt arrives, the service routine makes successive reads of one address of VXI memory. This address is read until the token is passed back to the ROC indicating that the last module has dumped all of its data. As a data word is read, it is broken into its two 16-bit components and appropriate addresses are incremented. At present each event increments three memory locations:

- A sum channel which is stored as the zeroth word of each histogram. The block offset determines the histogram number.
- The actual histogram address. The block offset determines which histogram and the time offset determines which channel of the histogram.
- A histogram that contains the sum of each of the data histograms is stored as the zeroth histogram. The block offset determines the channel in this histogram.

Two sum channels are maintained for each data histogram for convenience. The first sum described here provides some backward compatibility with our old system software and the second provides a mechanism for examining activity on a system level.

System Specification

Detector pulses from differential amplifiers are expected to be 1-2V pulses with decay times less than 1μsec. Each channel's upper and lower discriminator controls detector pulse height rejection. The 12-bit main board DAC provides the LLD. The DAC output operates at 2.5V full scale and provides LLD resolution of ~0.6mV. The upper level discriminator (ULD) is provided by a digital compare of the output of the 8-bit ADC on the SIMM with a threshold level stored in the FPGA. This ADC also operates at 0-2.5V full scale and so provides ~10mV ULD resolution. The value from the SIMM's ADC can also be used to provide a pulse height measurement for the detector by setting a software switch in the FPGA.

Instantaneous data rates are limited by a 1.5μsec lockout time in the SIMM's ADC. This imposes an instantaneous rate of ~666k-events/sec/channel.

Time average rates are limeted by the 2K word size of the Ping-Pong FIFO buffer on the TOF board. At 2K-events/33.333msec/module the data rate is limited to ~62k-events/sec/module or 3.8k-events/sec/detector.

Current Status

We have recently completed the final prototyping stage of the system for single element tubes. Communications with the data acquisition group at the Manuel Lujan Jr. Neutron Scattering Center (MLNSC) at Los Alamos National Laboratory during the development stage have led to a main board design that we believe can be used at both IPNS and MLNSC. We have procured parts for and have commissioned assembly of TOF modules for conversion of the HRMECS instrument. This conversion should occur during the winter of 1998. We plan, at this time, to adapt many components of the current data acquisition system (instrument computer, ancillary control equipment, control/setup software, etc.) with a more complete conversion as time and budget allow.

Future Plans

After the HRMECS instrument is converted to this data acquisition system and as time and budget allow we will convert the rest of the IPNS single element detector instruments to this system. During 1998 we should finish prototype work on using this module with linear position sensitive detectors. We should also start work on modules that will work with our area position sensitive detectors.

In the coming year we hope to move the system setup/control software to a new platform so that we can start to upgrade the instrument computers from the VAX systems that are currently being used. We are currently looking at Unix and Windows NT based computer systems as possible migration paths. As we

migrate the control software to a new platform we will be trying to provide a more intuitive graphical user interface and design a system that is independent of the chosen computer architecture.

The current IPNS DAS is implemented so that histograms for single element detectors must have constant time width bins (a means to allow channel width doubling after a defined number of channels was provided but never used). Unfortunately the intrinsic resolution of the instruments does not match this pattern. A system of compromise between resolution and available histogram memory has been adopted over the years. We will provide software in the near future for binning histograms in a pattern that more closely matches the resolution of the machine. For diffractometers this will mean constant $\Delta t/t$ time steps and for chopper spectrometers this will mean constant ΔE steps.

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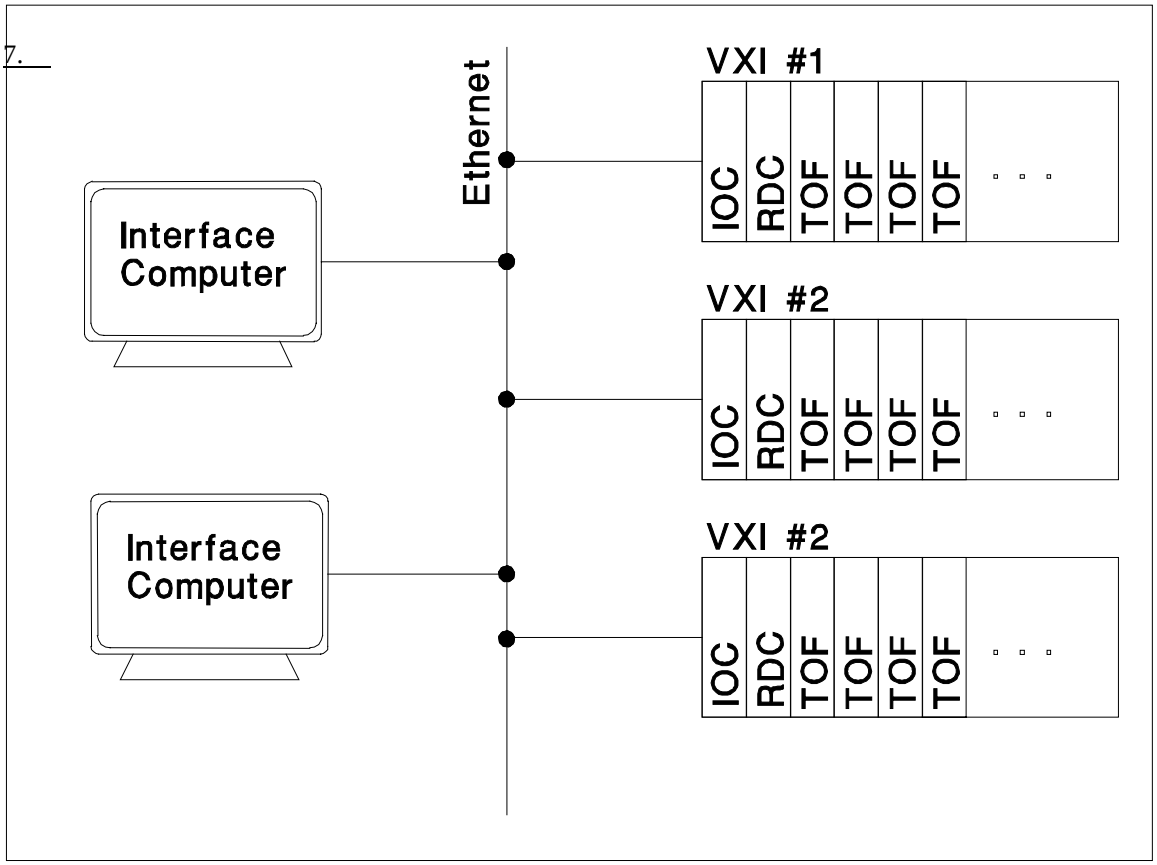

Figure 1 –IPNS Data Acquisition System Overview

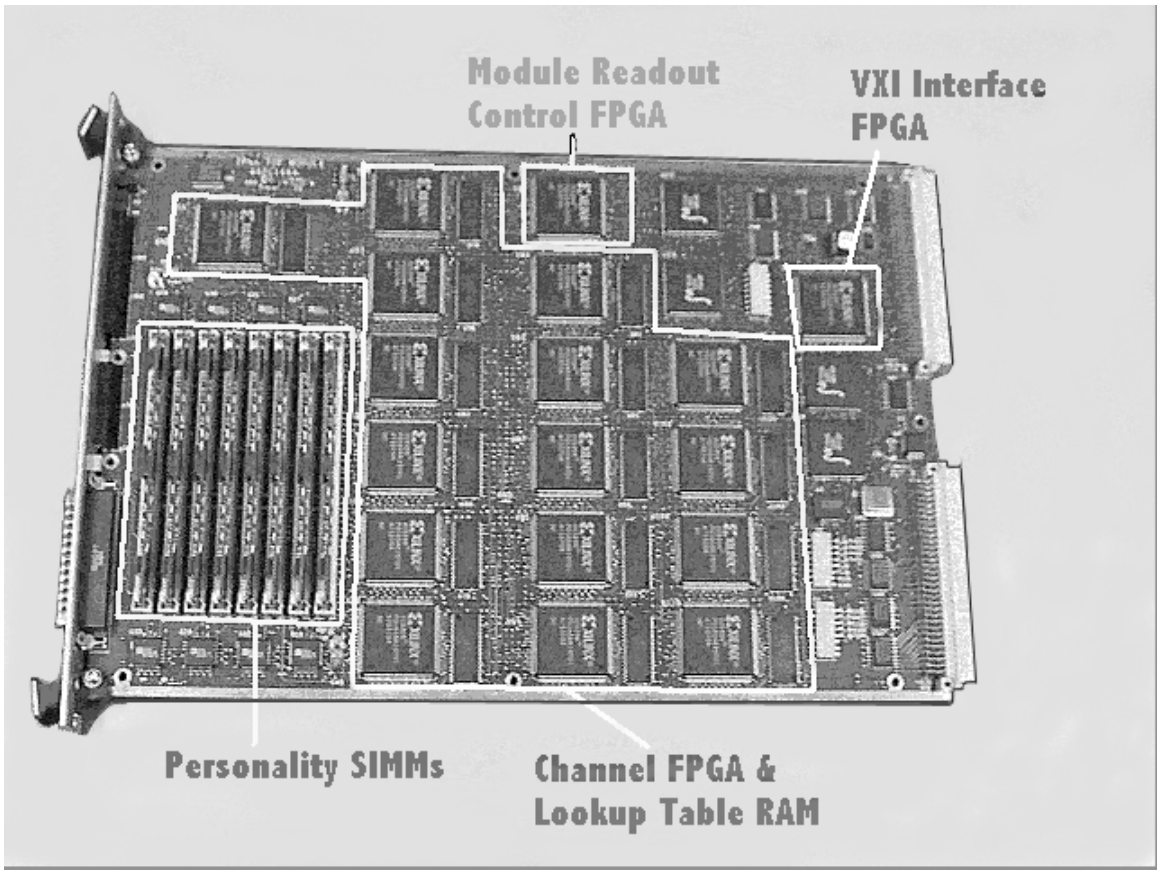

Figure 2 IPNS TOF Histogramming Module

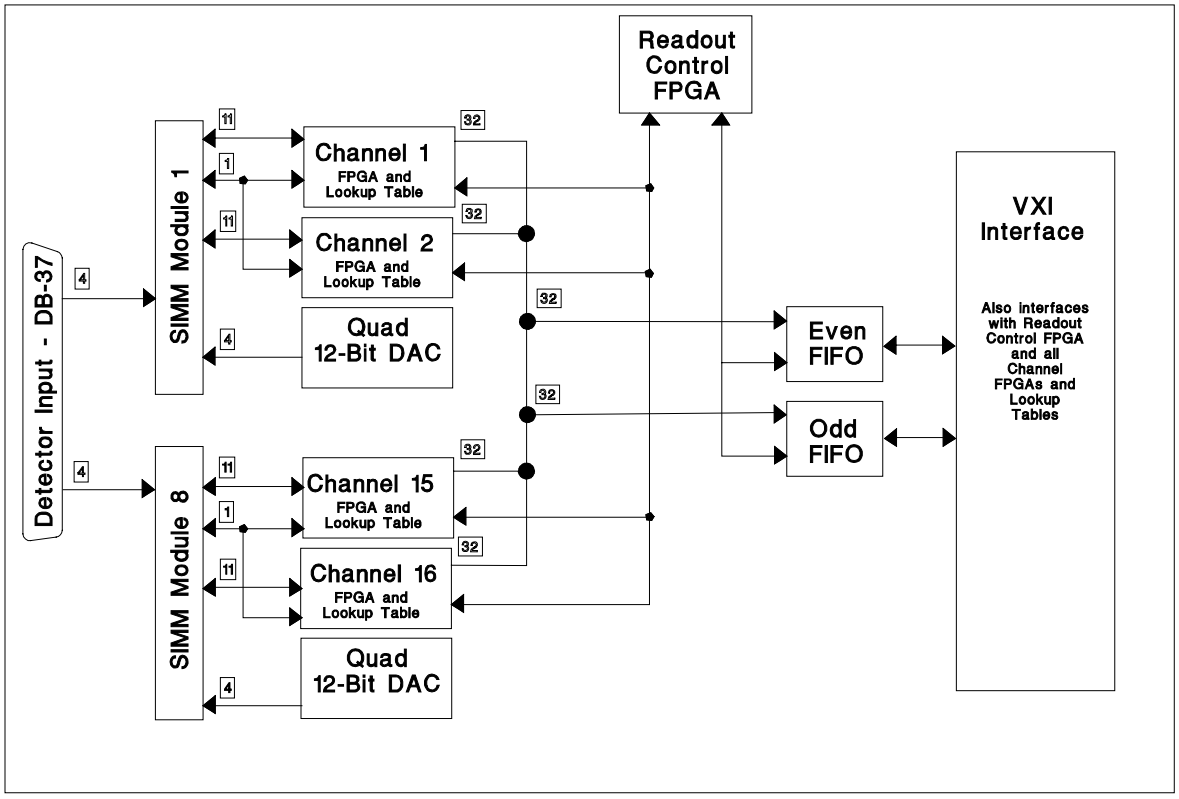

Figure 3 TOF Histogramming Board – Block Diagram

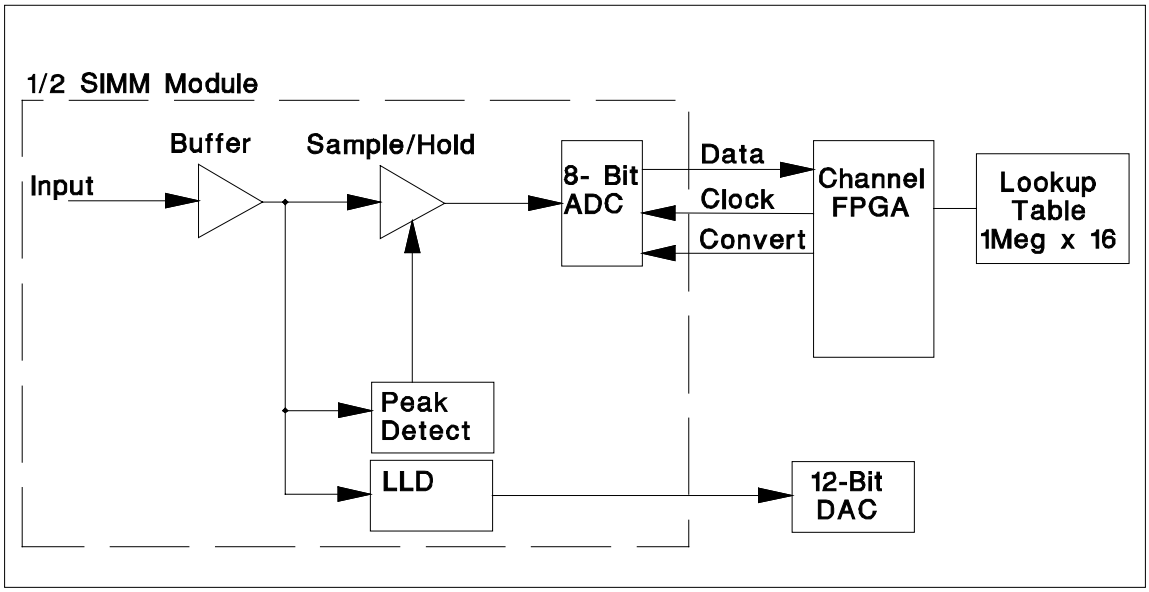

Figure 4 - TOF SIM Module, Block Diagram