Integration of Field Devices in a PROFIBUS Environment

H. Kleines, R. Madlener, K. Zwoll
Forschungszentrum Jülich GmbH, D-52425 Jülich, Germany

Abstract

Forschungszentrum Jülich (FZJ) introduced PROFIBUS to slow control systems in the context of physics experiments by developing a first generation of PROFIBUS controllers. These controllers are based on a microcontroller and just implement layers 1 and 2. Because of their limited performance and functionality, FZJ developed a new family of PROFIBUS controllers, in co-operation with an industrial company. The new PROFIBUS interfaces are based on the modern family of Siemens VLSI protocol chips. The whole range of protocol options without PA has been implemented. For simple, cost efficient adaptation of sensors and actuators a single chip solution has been chosen.

The paper will discuss the benefits of the diverse PROFIBUS options with respect to possible applications also in the field of experiment control. Central design decisions regarding hardware and software architecture will be discussed and a report of the experiences as well as first performance measurements will give an impression of the overall effort and possible problems.

1 Introduction

PROFIBUS, being a national German (DIN 19245 part I - IV) and an international European (EN 50170 Volume 2) standard, has become the most widely accepted fieldbus technology in Europe with more than 1000000 installed nodes [1]. A major reason for its success is the scalability in technology and functionality based on a common core. It is functionally scaleable by supporting dedicated, optimised protocol versions (DP, FDL, FMS, PA) and technologically scaleable by supporting designs based on a variety of protocol chips with different functionality down to pure software designs based on the integrated UARTs of microcontrollers.

Forschungszentrum Jülich (FZJ) takes the role of a user as well as a developer of PROFIBUS components. Developments have been undertaken always together with industrial companies. Therefore each described implementation can be used in industrial applications as well as in FZJ for experiment automation and control.

Because of the complexity of the PROFIBUS architecture, the selection of the appropriate PROFIBUS option for a given application scenario is a main issue. Also the variety of implementation options demands a careful analysis of the requirements.

2 The PROFIBUS protocol family and its implementation options

According to Fig. 1 PROFIBUS is defined as a collapsed architecture supporting layers 1,2 and 7 of the ISO reference model. For the optimised support of dedicated application areas, the three versions FMS (Fieldbus Message Specification, DIN 19245 part II), DP (Decentral Periphery, DIN 19245, part III) and PA (Process Automation, DIN 19245 part IV) have been defined around a common core, the Fieldbus Data Link (FDL, DIN 19245 part I).

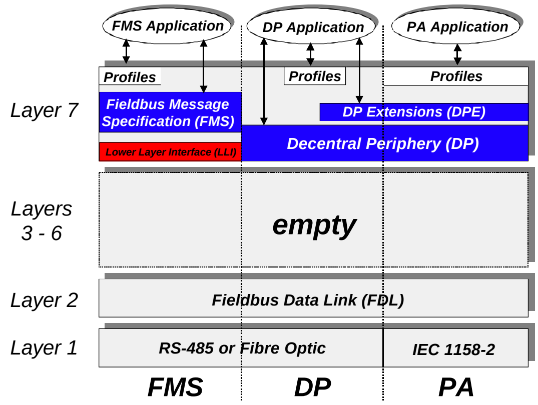

Fig. 1: The PROFIBUS protocol family[1]

PROFIBUS FMS is a universal communication protocol, primarily directed at the cell level for the communication between intelligent automation devices (e.g. PLCs). The FMS application layer is based on an object oriented client server model derived from the ISO MMS standard, which already incorporates automation functions [2]. Until now, the FMS protocol is rarely used due to its complexity and reduced performance compared to DP or FDL. But in larger process control applications it offers consistent semantics also down to the field level, thus simplifying design and configuration.

PROFIBUS DP has been designed for the optimised connection of simple, low cost I/O in a time critical environment. Typically, one master accesses the fixed I/O space of slaves in a cyclic way. So a DP system can be viewed as a distributed PLC. Most of the installed PROFIBUS equipment in industry follows the DP protocol, because it specifically fulfils the need for interfacing simple front end equipment [3].

The newest version **PROFIBUS PA** has incorporated results from the Interoperable Systems Project (ISP) and is specifically designed for process control applications in a explosion-hazardous environment [4].

FDL specifies a token bus protocol between masters with optional slaves. The direct access to FDL (without FMS or DP) often has been used in the early PROFIBUS applications but now it is being replaced continuously by DP.

Three transmission technologies are supported:

- RS 485 with baudrates up to 12 MBit/s,

- intrinsically safe physical layer according to IEC 1158-2 (H1 bus with 31.25 kBit/s)
- Fibre optic transmission

Several dedicated profiles have been defined in the context of FMS, DP and PA. A profile specifies the communication behaviour of dedicated device classes (e.g. PLCs, linear encoders, sensors, multiturn actuators), thus reducing the implementation effort and simplifying the exchange of devices from different vendors.

PROFIBUS is defined as an asynchronous protocol. Thus it was possible to implement a first generation of PROFIBUS interfaces based on microcontrollers in parallel with the development of the DIN standard. These implementations are purely done in software using the integrated UARTs without having to rely on any dedicated protocol chip. Today, there is a wide range of ASICs available (e.g. from IAM, Motorola, Siemens, DELTA t, Smar), allowing dedicated designs where high performance or offloading of the CPU are required. Complete slave designs purely in hardware are possible.

Because of performance, functionality and long term support the following Siemens devices - supporting baudrates up to 12 Mbit/s - seem to be most interesting.

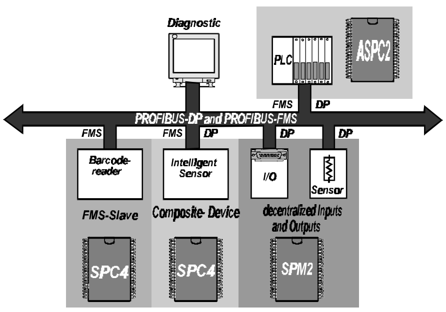

Fig. 2: Typical application field of the selected PROFIBUS VLSI controllers [5]

- **ASPC2:** protocol chip implementing the complete MAC layer of PROFIBUS. It supports the implementation of FMS master, FMS slave and DP master. Because of the missing baudrate detection the DP slave functionality is not supported.
- **SPM2:** single chip solution for simple DP slaves without CPU. It implements the complete DP slave functionality and contains a parallel interface (64 bit I/O) for directly accessing peripheral components.
- **SPC4:** protocol chip implementing the slave functionality of PROFIBUS layer 2 and parts of DP. It supports the implementation of FMS slaves and DP slaves. It can directly be interfaced with SIM1, a VLSI chip for the intrinsically safe physical layer according to IEC 1158-2, thus supporting PROFIBUS PA.

Fig.2 illustrates a typical application scenario incorporating all three ASICs in industrial control applications.

Together these ASICs support all possible protocol options of PROFIBUS. So they have been selected as the base of a new family of PROFIBUS controllers developed by FZJ.

The variety of hardware options is complemented by the availability of several portable protocol stacks for the individual ASICs and microcontrollers. Additionally, there is a variety of support tools (network analyser, configurator, etc.) available.

3 Requirements for a new family of PROFIBUS controllers

Forschungszentrum Jülich (FZJ) has implemented a family of first generation PROFIBUS controllers based on a microcontroller (NEC V25+) in order to introduce PROFIBUS in slow control systems for physics experiments and industrial applications [7]. Because of their limited functionality (just layer 1 and 2) and performance these interfaces are considered to be out of date. A modern design should make use of protocol chips and implement also the upper layers.

In order to avoid a major investment in a new family of interfaces, the core technology was implemented in co-operation with the industrial company Babcock Prozeβ-automation GmbH (BPA).

BPA manufactures a process control system as well as a scaleable family of multiturn actuators (BabcockMatic I, typically used for the adjustment of valves, based on a 4-20mA interface in combination with digital I/Os) and is experiencing a strong market pressure to provide PROFIBUS interfaces for their actuators as well as for their process control system.

So the basic design decisions for the PROFIBUS controller of the actuator had also to take the following requirements of BPA's process control system into account:

- support of FMS and of DP,
- PROFIBUS master functionality,
- PROFIBUS slave functionality for low cost designs.
- high performance,
- the CPU of intelligent controllers should be compatible to Motorola 68K CPUs, because they are used in the automation layer of the process control system.
- redundancy [6]

Besides redundancy all defined options are required by PROFIBUS applications inside FZJ, including slow control of experiments as well as remote monitoring and control of embedded CPU systems and power supplies like CAMAC, FASTBUS and VMEbus. In the context of slow control systems the new family of PROFIBUS controllers connects our specific equipment to the open world of industrial modular board systems (e.g. SMP), PLCs, sensors and actuators [7].

4 Design of the new family of PROFIBUS devices

4.1 FMS/DP-master interface

The requirements listed in the previous sections demand the implementation of a DP/FMS master based on a powerful microcontroller and protocol chip for the MAC layer. Here the Siemens ASPC2 was selected because of performance and support. The existence of a portable PROFIBUS protocol stack and the 68K-compatibility lead to the microcontroller MC68340.

In order to use the PROFIBUS controller in variety of applications and configurations and due to space limitations, it was designed as a modular system of two directly connected boards. One board contains the base controller with CPU logic and PROFIBUS part, the other one is a peripheral board containing components like ADCs, DACs and binary I/Os, which do the interfacing to the actuator. An additional peripheral board for PCI bus has been developed on the base of the AMCC S5933 PCI Controller and a Dual Port RAM (8K*16) for the transfer of messages between host and controller.

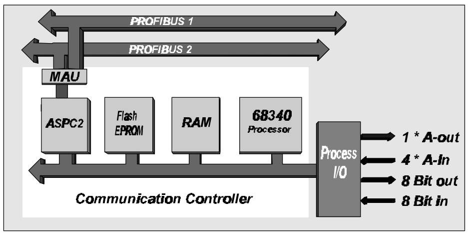

Fig. 3: Block diagram of the PROFIBUS controller (core and peripheral board)

As usual, the base controller is implemented as an intelligent subsystem according to Fig. 3, with a central address/data/control bus connecting the CPU MC68340FE16, 256 KBytes FlashEPROM, 256 KBytes of static RAM and the ASPC2. For the simultaneous support of FMS and DP the FlashEPROM has to be increased to 512 KBytes. The control logic contains reset logic, a watch dog timer and the redundancy support [6]. The CPU is a microcontroller containing all required peripheral components like interrupt controller, timers and UARTs and has a programmable clock rate which has been tested up to 16 MHz, the value used here. A dedicated medium attachment unit supports a redundant cabling system.

The portable protocol software was acquired from the German company Softing and adapted to the new hard-ware. The application software, which maps PROFIBUS services to interactions with the actuator, was implemented as a task under control of the board level operating system kernel SOS (Softing Operating System). SOS was delivered by Softing as an execution environment for the modules of the protocol stack, thus offering a standardised interface for accessing the services of FMS, FM7, DP and SOS.

4.2 Implementation of the DP slave interfaces

In order to achieve a cost-efficient design, a DP slave version for the actuator interface without CPU was developed. It is based on the SPM2 with some glue logic for accessing the "ident number" and the PROFIBUS address of the station as well as the analogue and digital I/Os for interfacing the actuator (Fig. 4). PROFIBUS part and peripheral devices could be integrated on one board. Of course, there was no software development effort on the PROFIBUS interface, at the cost of a little bit higher software complexity in the master. So this approach is considerably cheaper than the FMS/DP master.

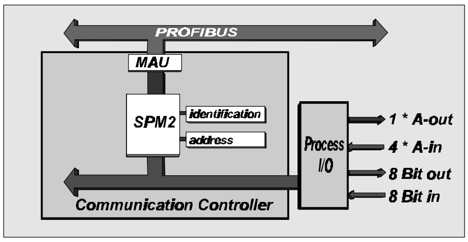

Fig. 4: Block diagram of the simple DP slave [8]

In order to have some intelligence in the front end (e.g. for statistics or calibration), also an intelligent DP slave based on the SPC4 was implemented. By using a similar design as for the ASPC2 based board, basically by replacing the ASPC2 with the SPC4, a maximum synergy regarding hard- and software development could be achieved.

5 Performance measurements

In [9] extensive measurements of FDL and FMS have been presented based on the standard user method and hardware monitoring. The measurements concentrated on the overall performance characteristics exhibited to the user application and Fig. 5 summarises the results together with new measurements of DP.

At the individual layers the minimum response times for the following acknowledged services have been measured:

- DP: *data_exchange* service (based on FDL service SRD)
- FMS: *read* service (based on FDL service SDA)
- FDL: *SDA* service (Send Data withAcknowledgement)

Fig. 5 shows that the use of protocol chips leads to a major decrease of response time (Factor of 5 between old and new design at FDL layer). This is mainly due to the fact, that the responses of at DP and FDL are generated completely in hardware. So we measured that the "reaction time" of the chips (e.g. Time between incoming and outgoing token, incoming SDA request and outgoing SDA acknowledgement, etc.) is basically identical with the setting of the timer min_tsdr (minimum station delay responder). Minimal settings of min_tsdr are 11 bit times for the SPM2 and 17 bit times for the ASPC2, thus depending on the baudrate (e.g. 22µs and 34 µs at 500 kBit/s). Because the reaction times of stations, especially the token transfer time are a crucial issue for each token passing protocol, the main advantage of the use of the chips is the dramatic increase of overall bandwidth on the bus. This gets especially evident when considering, that the reaction time of a pure microcontroller based implementation is in the order of 0,5 ms with a maximum baudrate of 500 kBit/s (instead of 12 MBit/s). The effect of the baudrate on response time is determined by the physical transmission time on the medium. So it can be computed directly and is neglectable for small message sizes. Because of the inherently low degree of parallelisation, this holds also for the throughput between two stations, as shown in [9].

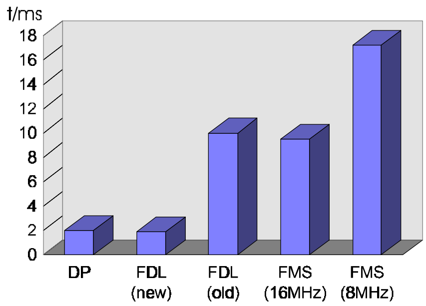

Fig 5. Minimum Response Time *t* in various PROFIBUS configurations measured at 500 kBit/s

So the overall response times are basically determined by software delays. This gets especially evident when looking at FMS. Here we measured, that the response time is almost proportional to the CPU clock.

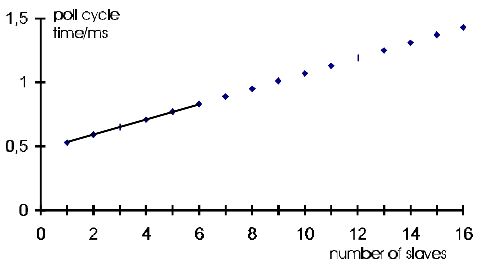

Fig. 7: Poll Cycle duration measured at 6 MBit/s

DP exhibits its strength when one master accesses several SPM2 based slaves in a cyclic mode. In this mode, the data exchange does not occur on explicit request of the application, but asynchronously to/from a dual ported memory, leading to a major speed up. Fig. 7 shows cycle duration (including read and write operation at each slave) measured for 1,2,...,6 slaves at 6 MBit/s and extrapolated to 16 slaves.

6 Conclusions

The PROFIBUS architecture provides a variety of options for dedicated application areas. So, a careful analysis of the communication requirements of an application is a key issue for the implementation of a an application based on PROFIBUS. This leads to an appropriate selection of options as well as available hardware and software components, thus optimising costs, maintenance effort, performance and integration effort. The developments of FZJ represent optimised designs for all protocol options of PROFIBUS, apart from PA. For interfacing simple slave devices the SPM2 solution should be the preferable solution. Otherwise, additional firmware has to be integrated in the devices, leading to more complex systems.

Measurements showed, that the increase of the overall bandwidth in a PROFIBUS system is a main advantage of modern PROFIBUS ASICs. In addition to this, extremely short response times can be achieved when accessing SPM2-based DP slaves in a cyclic mode. Because of the hardware support for DP, it can be assumed that also SPC3 and SPC4 provide similar response times. But this assumption must be proven by future research.

References

[1] http://www.profibus.com

[2] S.W. Zhang: "Fieldbus technology overview and its impact on industrial automation", FieldComms USA, Boston, June 1997

[3] M. Deppe : "Anforderungen an ein modernes Feldbussystem - Was bietet PROFIBUS DP", iNet 95, Karlsruhe, Juni 1995

[4] A. Schimanski: "Profibus PA Field Instrumentation", FieldComms UK, November 1996

[5] "PROFIBUS Technische Druckschrift", PROFIBUS Nutzerorganisation e.V, Oktober 1995

[6] H. Kleines, R. Madlener, J. Holzer, K. Zwoll: "Implementation of a redundant PROFIBUS-Interface for an industrial Actuator", FieldComms Europe, October 1996

[7] K. Zwoll, H.-J. Eisenbach, J.L. Sarkadi: "Open Fieldbus Communication (PROFIBUS) in Physics Experiments", Real Time Data '94, Dubna, Russia, June 1994

[8] D. Becker: "Entwicklung einer Anschaltung an ein Feldbussystem auf der Basis von PROFIBUS-DP", Diplomarbeit FH Aachen, 1996

[9] H. Kleines, R. Madlener, J. Holzer, K. Zwoll: "A universal Family of PROFIBUS Interfaces for Process Control Applications", Fieldcomms USA, Boston, June 1997