Upgrade Plan for the NSRL Control System

Wei-Min Li, Shou-Ming Hu, Jing-Yi Li and Yong-Bin Leng
Hefei National Synchrotron Radiation Laboratory
Song-Qiang Liu*
Department of Modern Physics
University of Science and Technology of China, Hefei, Anhui, 230026, P.R.China
[1]

Abstract

The control system of Hefei National Synchrotron Radiation Laboratory (NSRL) was designed in 1983 and completed in 1990. In the present system, the device controller is a MULTIBUS-I based system with 8085 processors, which is star-networked to the high level computer through a communication controller. An 80486 PC is used for both high level control and operator interface.

The upgrade of NSRL control system will start at the end of 1997 and last about 3 years. The new control system will be EPICS based, following the standard model, i.e. I/O controllers (IOC) communicating via Ethernet with operator interface workstations (OPI). Both MVME162 and PC will be used as IOCs and CANbus will be used for the communication between IOCs and the device controllers.

1 Introduction

1.1 NSRL overview

Hefei National Synchrotron Radiation Laboratory (NSRL) is controlled by the Chinese Academy of Sciences and managed by the University of Science and Technology of China. The NSRL consists of a linear accelerator , transport line and electron storage ring. The electrons are produced by an electron gun and accelerated to 200 MeV in the linear accelerator, then transported to the storage ring and ramped to 800 MeV. After ramping, the electrons circulate around the storage ring as a stored beam at the energy of 800 MeV. The central part of the facility is the 800 MeV storage ring, which has an average diameter of about 21 m, placed in a 50 m diameter hall. The facility produces synchrotron radiation ranging from soft X-rays to ultraviolet light. Five beamlines have been in use for many years and 8 beamlines will be added in the coming Phase-II project.

1.2 The existing control system

The control system of NSRL was designed in 1983 and completed in 1990[1]. The backbone of the existing system is the main power supply control system, as shown in Fig. 1. The power supply controller is a MULTIBUS-I based system (with 8-bit 8085 processors) which is star-networked to the high level computer through opto-coupled RS-422 links and the communication controller. Originally the high level computer was a PDP11, in 1992 the PDP11 was replaced by an 80486 PC which is used for both control and operator interface.

There are some problems with the present control system. First, there is no connection between subsystems (such as power supply control, vacuum monitoring and radiation safety monitoring, etc.) thus they can only be operated independently. The second problem is with the software development and maintenance because of the shortage of manpower. In fact, we have been using a set of simple and crude software tools since 1990. The last problem is that the hardware components are out of date and maintenance is becoming more and more difficult.

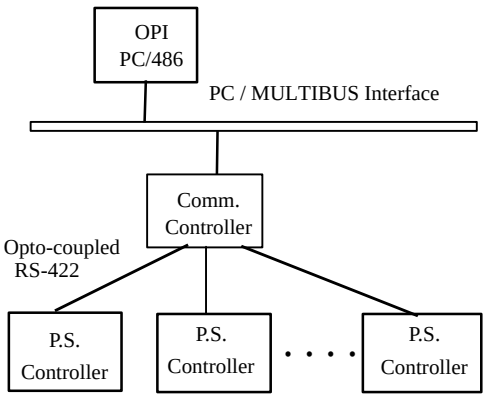

Fig. 1 NSRL existing main P.S. Control System

2 System upgrade

2.1 Upgrade plan

As a part of the Phase-II project, the upgrade of NSRL control system will start at the end of 1997 and last about three years. The new control system will be EPICS based, following the standard model of I/O controllers (IOC) connected to workstations (OPI) via Ethernet. The system architecture, shown in Fig. 2, includes the following subsystems:

- ring main power supply control and monitoring.
- ring correctors power supply control and monitoring.
- linac and transport line quadrupoles and correctors power supply control and monitoring.
- vacuum monitoring.
- temperature monitoring.
- radiation safety monitoring.
- RF cavity control and monitoring.
- closed orbit feedback system.

*Corresponding author[1]

For most subsystems the secondary (remote) I/O system is necessary. For economic and practical reasons, in these

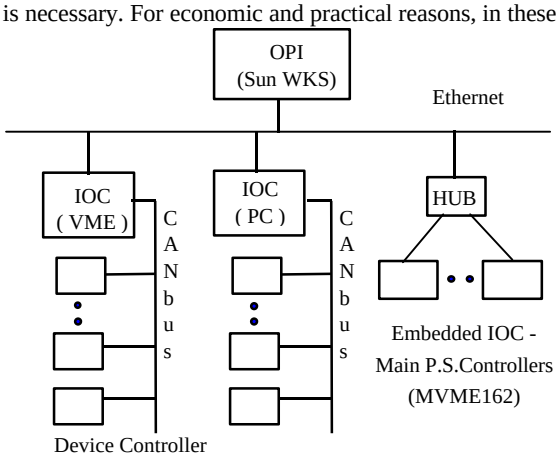

Fig. 2 NSRL New Control System

systems the processor of the device controller will be a 16 bit microcontroller. CANbus will be used for communication between the IOC and the remote controllers not only because of its excellent performance but also because it is already supported by EPICS[2][3].

The main power supply control system is more complicated, we will develop new main power supply controllers by using MVME162 together with IndustryPack modules. Since EPICS supports MVME162 as an IOC, we would directly use the P.S. controller as an embedded IOC, this will be discussed in next section.

Since VxWorks supports PC as a target and EPICS supports PC as an IOC, we would like to use PCs as IOCs for some subsystems.

2.2 Upgrade steps

In order to minimize the impact on machine operations, the upgrade of the control system must be done in step.

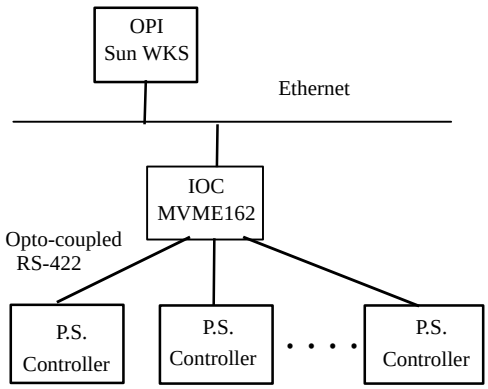

Fig. 3 the first upgrade step

At the beginning we would like concentrate our effort on the upgrade of main power supply control system. First we will build a basic EPICS system for the main power supply control, as shown in Fig.3, keeping the existing MULTIBUS-I based P.S. controllers and its RS-422 communication protocol. The IndustryPack module IP-Octal Opto-RS-422 will be used to link the IOC with the P.S. controllers.

Eventually new MVME162-based main P.S. controllers will take the place of the old MULTIBUS-I based P.S. controllers and the RS-422 link will be removed.

Once the upgrade of main power supply control system is completed, other subsystems will be added one by one to this basic EPICS system.

3 Upgrade of main power supply control system

3.1 The existing main power supply control

NSRL has 11 main power supplies: 1 for ring bending magnets, 8 for ring quadrupole magnets and 2 for ring sextupole magnets. All of these power supplies work in ramping mode. In the existing main power supply control system[4] each power supply is controlled by a MULTIBUS-Ibased power supply controller, which consists of a 80/24 CPU module with an 8-bit 8085 processor, a 16-bit DAC module and in-house developed Ramping and Communication modules. Because the P.S. controller is separated from the power supply and its DAC output is sent to the power supply through a cable several meters long, the system suffers from EMI problems.

3.2 Hardware configuration of new main P.S. controller

The main power supplies work in ramping mode during injection, so the controller's processor should be more powerful to provide floating point capability for linear interpolating ramp tables in real time. On the other hand, since our's is a small system (only 11 power supply controllers) , we prefer that all the hardware components of the controller be commercially available to reduce the hardware and software in-house development to a minimum. For these reasons MVME162 and IndustryPack Modules have been chosen to build the main P.S. controller. Fig. 4 shows the functional block diagram of the main power supply controller, which consists of the following modules:

- MVME162 VME module controls the power supply through a set of IndustryPack I/O modules.
- IP 16 DAC module used to output waveform to control the power supply. According to the specification this module has internal deglitching hardware which produces a faster settling time and is suitable for high resolution waveform generation.
- IP 16 ADC module with 8 differential 16-bit ADC channels. One channel is used to acquire the high resolution value from the DCCT, other channels are used to monitor the PS voltage, temperature etc..
- IP UniDig-I-D module with 24 flexible digital I/O channels for controlling P.S. and monitor P.S. status.
- There will be an extra IndustryPack module IP UniDig-T-D in the bending magnet P.S. controller, which provides count down timers and will be used to provides a step signal to synchronize the ramping of the power supplies.

The main power supply controller will be mounted in a

chassis built into the power supply crate.

3.3 Embedded IOC

Conventionally, EPICS IOC is at the primary IO level and the power supply controllers are at the secondary (device) level, one IOC controls several power supply controllers through fieldbus. Because MVME162 is chosen to be the main P.S. controller and EPICS supports it as an IOC, naturally we can simplify the design by directly using the MVME162 as the IOC as well as the power supply controller. Thus, each main power supply is directly controlled by an embedded, MVME162-based IOC.

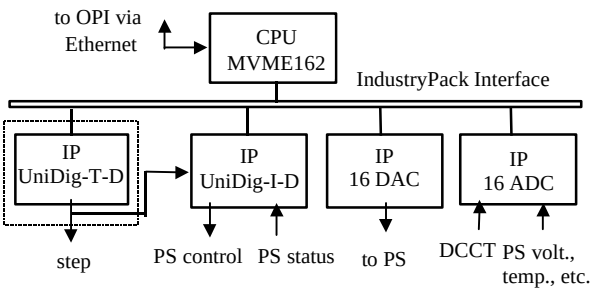

Fig. 4 Embedded IOC / Main Power Supply Controller

References

[1] Yao Chih-Yuan, ICALEPCS, KEK, Tsukuba, Japan, 1991, p.40
[2] M.Clausen et al., ICALEPCS, Berlin, Germany, 1993, Nucl. Instr. and Math. A 352 (1994), p.19
[3] J. Bergl et al., ICALEPCS, Chicago,USA,1995, p.1017
[4] C.Yao et al., Proc. Int. Conf. on Synchrotron Radiation Applications, Hefei, China, 1989, p.237