Using Reconfigurable Processors as Control System Elements

Timo Korhonen, Adrian Lawrence*, Ian Page*, Junji Urakawa
KEK, High Energy Accelerator Research Organization
Oho 1-1, Tsukuba, Ibaraki 305, Japan
*Oxford University, Computing Laboratory
Parks Road, Oxford, OX1 3QD, United Kingdom

Abstract

A control system applying reconfigurable computers has been designed and built for the active alignment system of ATF at KEK. The system measures the relative position of accelerator components with a high precision allowing remote correction of the misalignments. A control system that acquires the data and permits the position control was developed. The system was built using reconfigurable logic as processing elements. To program the devices, a hardware compiler was utilized. The system structure, divided into functional levels and the tasks and processings done at each level is reported.

1 Introduction

The ATF (Accelerator Test Facility) at KEK has been built with the purpose of studying the techniques and phenomena related to building a linear collider. The principal components of ATF are a 1.54 GeV injector linac and a 1.54 GeV damping ring. One of the primary goals of the accelerator is producing ultra-low emittance beams in the Damping Ring (DR). To achieve this goal, the accuracy of the alignment has to be in the range of tens of microns [1]. An active alignment system, with the purpose of keeping the components of the damping ring constantly aligned by compensating for the floor motion, has been built for the ATF.

The control system for the alignment system utilizes reconfigurable processors; logic devices that can be dynamically programmed for specific tasks. The key techonology that makes the programmable logic feasible as processing elements is hardware compilation. We use the Handel compiler [2], developed at Oxford, to program the logic arrays. The compiler makes the programming very much simpler than using contemporary tools, as the hardware details need not to be worried about. The computing circuit is generated from source code so the computing can be performed very fast.

2 The active alignment system

The ATF damping ring has a racetrack shape. The accelerator components in the circular arc sections are placed on controllable tables (movers). The tables can be precisely controlled in five degrees of freedom: horizontal and vertical, roll, pitch and yaw. There are a total of 36 mover tables, 18 in each arc section. The tables are positioned in 10 degree angles relative to each other.

In a circular accelerator it is not practical to use a global reference, so a method that depends only on a few reference points is required. To measure the relative position of the tables in ATF, diode lasers used as light sources are mounted on the end of one mover table and detectors to measure the position of the light spot on the end of the neighbour table. Using a combination of two-dimensional position detectors separated by a suitable distance we can measure position in five degrees of freedom. The position information is shared between the tables through the control system.

3 Control system

A data acquisition and control system is required for handling the measurement data and controlling the movers. The system has to be connected to the main control system of the ATF so that the information can be shared with other components of the control system.

CAMAC [5] is an extremely robust and well established standard and still in wide use. However, the standard is showing its age. It is quite hard to include new features like intelligence at the low level and distributed features. The ATF control system is based on CAMAC for a variety of reasons. A major part of the required hardware components and some basic software for the control system were readily available.

Using the CAMAC system only, all the I/O operations would have to go through the central computer. It seems reasonable to have an intermediate layer to ease the burden of the central control system. To build such a system there are several possible approaches. The most obvious one would be to use some kind of fieldbus interface to the CAMAC system and microprocessors to drive the local controllers. This kind of solution would have the flexibility that is needed. However, it is not so easy to find an interface that could be readily integrated into our system.

3.1 Hardware/Software codesign

The performance of programmable circuits is increasing rapidly. The RAM-based field-programmable gate arrays (FPGA) can be dynamically reconfigured, which makes them ideal for custom computing devices.

The logic design for the programmable devices can be done either using schematic capture or a behavioural description like VHDL. A more recent approach is to use a

hardware compiler to generate the circuit from a program source [2]. The programming language approach has numerous benefits: it enables the use of an algorithmic approach even in the lowest-level tasks. The borderline between software and hardware is moved all the way down to the digital interface. No detailed knowledge about the hardware is necessary to use the circuits.

In the ATF system the Handel language [2] is used. The design of the Handel language is based on a sound mathematical theory of Communicating Sequential Processes [3]. Handel semantics makes it possible to follow and control the temporal behaviour of the hardware. The programmer can rely on the hardware implementation to work as written in the software and even verify that the behaviour is correct.

When programs run directly on hardware the algorithms do not need any interpreting level and can be very fast. It is possible for example to integrate a signal processing algorithm directly into the low-level hardware, or embed sensor data validation into the driving circuit itself [4]. A general overview of hardware compilation in sensor applications is given in [7].

4 Control system architecture

The control system has to bind together a mix of sensor and control hardware and integrate them into an existing control system framework. Reconfigurable computers are used to glue the components together and to bring computing power to where it is needed.

To achieve the proper task distribution, a three-layer structure was adopted (see figure 1). Each layer is provided with the required kind of computing capability. The lowest level has to have abundant I/O but the computation is fairly straightforward; the middle level needs no direct IO but has to have network connections and a moderate capability to do floating-point calculations. The top level is concerned with the alignment and monitoring and does not need to know about the processing done in the lower levels. The top level uses the facilities of the global ATF control system; the implementation of the lower levels is totally transparent to this layer.

4.1 Hardware interface layer

The lowest level communicates with the sensor and control hardware and processes requests from the upper layer. The tasks are performed by FPGA-based processors that are programmed in Handel. The controller for one mover table reads in the data from three analog-to-digital converters (ADCs), relays communication data to and from the mover controller through an RS-232C serial port and handles a set of digital I/O ports (figure 3). The communication link is used to transfer the data to upper level.

For the processing, the Accelerator Card from Embedded Solutions Ltd. is used [11]. The card has no traditional processors but instead two FPGAs (Xilinx 3195A). One FPGA (master) is connected to a communication link driver that enables remote configuration and communication using the board. The second FPGA (slave) has 22 of its pins available for external input/output. The two FPGAs are connected with a data bus for communication between them. External circuits are driven through the FPGA and normally do not need any intermediate logic. This makes the hardware very simple; the number of components is reduced to a minimum.

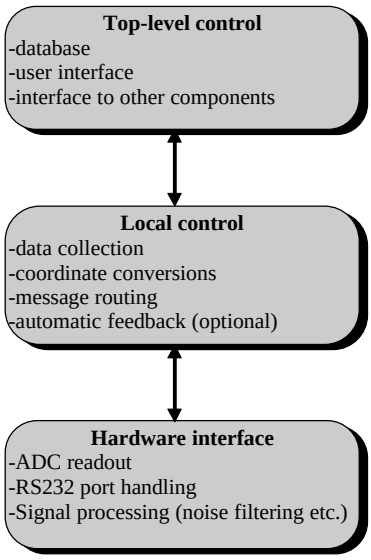

Fig. 1 Control system architecture.

The software is simplified because there is no need to worry about complexities like handling interrupts, multiple processes and similar things that would be required in the case of using a regular CPU. The simplicity makes it easy to guarantee the robustness of the processors, as all of their behavior is contained within the Handel-C code.

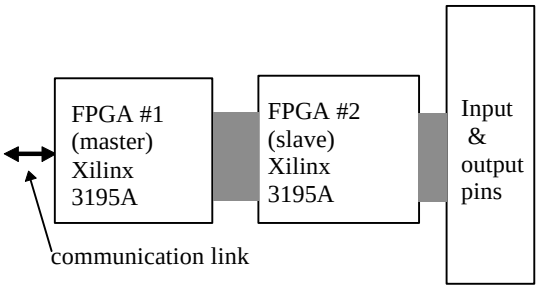

Fig. 2 The Accelerator Card block diagram.

The software of the low-level processor nodes responds to requests from the upper level to access the hardware, for example to read the value of one ADC channel. One processor unit handles several kinds of hardware and the requests and data have to be addressed to the right unit. This can be achieved by employing a simple protocol. The ADC′s are driven through a serial interface to minimize

the required pin count. After receiving a request to read an ADC channel, the software has to drive the serial interface. For RS-232C communication and digital I/O there are also corresponding subroutines that are called in reply to the incoming requests.

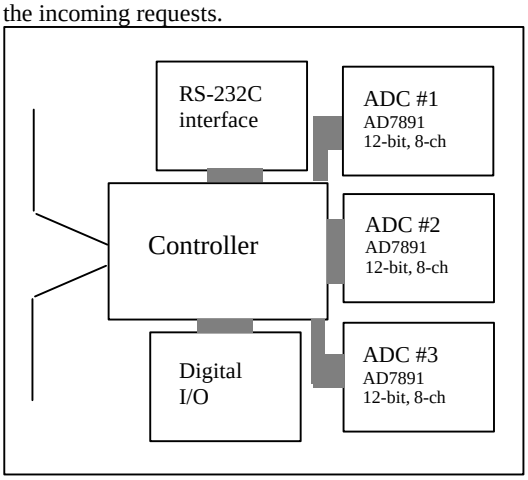

Fig. 3 Hardware level processor functions.

There is still room for addition of more elaborate tasks. For example, employing a constant monitoring of the light intensity could be used to implement an interlock system to detect too large movements of the tables that could cause harm to the vacuum system.

4.2 Local control network

At the next level the hardware is bound into a local control network that can be handled from a single CAMAC connection. All the commands and data are routed through this network. The data from the lower level is gathered and the necessary normalizations and corrections are applied to convert the raw values into physical units of displacement.

The SMT-219 board [8] is used as the main processor of the local control. It includes a T805 transputer processor, a Xilinx 3195A FPGA and 4 MB of RAM that is shared by the T805 and the FPGA. The T805 has four 1.5 MB/second serial communication links that are used to connect the subprocessors.

The SMT-219 is inserted in a module and the CAMAC signals are connected to the FPGA. This module is used as the interface between the CAMAC bus and the local control network. The module is very simple, consisting only of buffer circuits and a simple digital logic to enable bootloading the SMT219 through the CAMAC bus. The logic is active after a power failure or a hardware reset and is disabled after the FPGA has been configured.

The FPGA is programmed to run the CAMAC protocol. It can access the common memory using direct memory access (DMA). The T805 gathers the data from the network into a memory block which is accessible through the CAMAC bus. For the commands to be sent to the processor network, the FPGA stores the command into the common memory and then informs the processor about the command by sending it an event signal.

To gather the data into the common memory, the T805 CPU sends data request packets on the local control network. Each processor node on the network has a private address. Using the address information on the received packets the root CPU can order the data into the memory block.

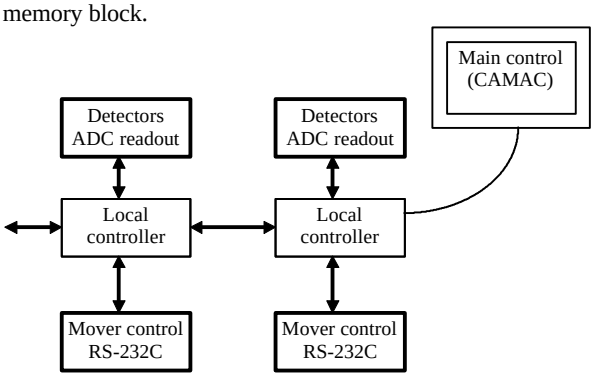

Fig. 4 (Local) control of the Active alignment.

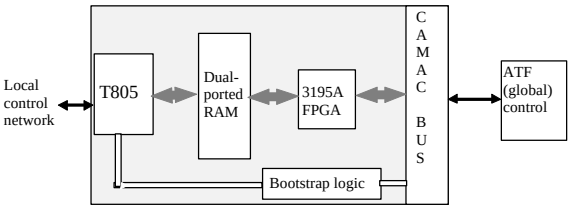

Fig. 5 Block diagram of the CAMAC interface

4.3 Top level control

The top level controls one component of the ATF control system rather than a separate subsystem. Its purpose is to integrate the active alignment with the other components of the ATF.

The ATF main control system [12] is built using the Vsystem [9] control software tools. To make sharing of data between the subsystems possible, the data is kept in Vsystem real-time databases. The data from the alignment subsystem is also stored in a database to make the data sharing simple.

The real-time databases hold the current values of data, whereas the data from the measurement system is inherently time series data. The database has to be periodically accessed and the data saved to create a time series file. This can be done by either a special purpose program or using the Vlogger tool. The time series data can then be accessed with other tools and programs.

5 Conclusions

Reconfigurable processors have been applied to the ontrol of the active alignment system of the ATF damping ring. Use of the reconfigurable processors made it easy to match the computing tasks with the functional division of

the system. All the low-level control tasks can be accomplished by the use of a single module. With the proper software, this module can take over tasks that used to need the development of additional hardware for each task. Handling of ADCs, serial communication, digital IO and so on can be done in a single circuit. Adding functions or changing the interface can be done instantly, even without stopping the operation of the rest of the system.

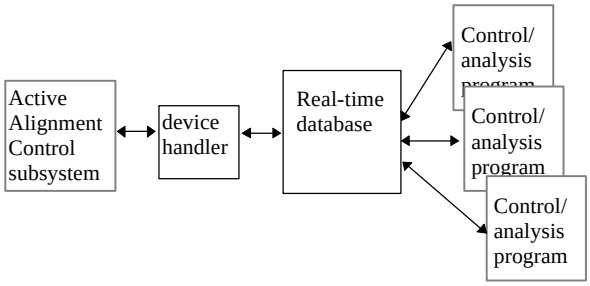

Figure 6. Top level control block diagram

The use of reconfigurable computers allows us to use the concept of ′virtual hardware′. By analogy with virtual memory on microprocessors, it is possible to download new hardware configurations at run-time, thus changing system behaviour. This may be useful if it is found that different control regimes suit different operating conditions that might arise during operation.

In a large-scale system the cost advantage of reducing the number of modules and module types to stock could be large. The risk of some components like a CPU design becoming obsolete could be avoided. The work done on software can be protected; even if the detector hardware is changed, it can be made to look similar to the software. At the moment, the relatively high cost of FPGAs however offsets the cost advantage. However as FPGA prices are dropping rapidly, this is fast becoming a serious alternative.

For low-level control systems that interact with the hardware, combination of reconfigurable computers with a fieldbus standard will undoubtedly become a reality and will be useful for many control tasks.

For our application, the main advantage of this approach lies in its flexibility: new technology can be incorporated while retaining the compatibility with the present system.

Acknowledgments

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The movers and the position measurement system are essential components of the active alignment system. However, the space does not allow them to be presented here and here we just want to acknowledge the efforts of the people that were involved in the development. These parts will be reported separately.

Parts of the hardware were developed in the Computing Laboratory, in collaboration with the Control Engineering Group in the Department of Engineering Science, University of Oxford. The Accelerator Card was re-engineered and commercialized for our project by Embedded Solutions, Ltd. Their efforts and contributions are greatly appreciated.

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