Advanced DSP-Based System Architectures for Data Acquisition and Control

V.I.Vinogradov, INR RAS, Moscow, RF
Email: vingradov@al20.inr.troitsk.ru

Abstract

Distributed data processing systems with single-chip microcomputers open new possibilities for system development, including embedded single-board systems and distributed network-based systems. The main problem is to select optimal microcomputers and develope efficient approach to modern System Architecture. One of the optimal approaches should give the way to upgrade a lot of existing systems to modern requirements and to develop a compact new generation systems on the base of the same micromodular subsystems fragments. The selected single-chip fix- and floating-point micro-computers /1/ should have a flexible I/O with Internal DMA (IDMA) to get a high-bandwidth systems. Each system node can have a SMP possibility and flexible interfaces for Interconnections. Distributed memory approach to RT-System Architecture of Data Acquisition and Control can be based on single or multiprocessor fragments and Interconnections with PC .

As example of the compatible upgrade (up to 30-60 MB/s) of existing systems on the base of fix-point DSP-based fragments in distributed modular RT-Systems are proposed (FASTCAMAC). The New generation compact multi-processor micromodular systems with Distributed Memory Overlayed Architecture and fragmented DSP and micro-computer based RT-Systems are proposed and discussed. The simplified SCI-type Interconnection for low-cost RT-Systems are proposed and discussed.

1 Problems of distributed memory RT-systems

Comparative analysis of the modern requirements and System Interconnections shows new problems and ways to get best results in development of efficient RT-systems on the basis of new technologies. Distributed data processing systems with single-chip microcomputers open new possibilities in system development, including embedded DSP-based multiprocessor single-board RT-systems and some distributed network-based systems. The main problem is to select optimal microcomputers and efficient approach to modern System Architecture. One of the optimal approaches should give the way to upgrade a lot of existing systems to modern requirements and to develop a compact new generation system on the basis of the same micromodular subsystems fragments. The first main problem is selecting the advanced DSP-based Core fragments for RT-Systems and interface between microcomputer modules and PC. The second basic problem is to develop efficient Distributed Memory Architecture and construct efficient System Interconnections. The modern PC is good instrumentation (platform) for new System Integration and user interface.

Analysis of high-speed DSP and new principles of Bus and Non-Bus Interconnections in modular systems shows the great possibilities in compatible high-speed extension of existing modular systems (FASTCAMAC) with DSP and networks Interconnections (FASTETHERNET) with Integrated Communication Processors (ICP). Micro-modular multi-processor structures on the board and development of Distributed Memory System Architecture with efficient Interconnections should be based on a single-chip core fragment for System Controllers (SC), Interfacing with modules in target RT-Systems and Personal Computer (PC).

Proposed Overlayed Architecture is optimal for RT-Systems, because of no time is spent on data transmission between memories of microcomputer modules. The transfer time is reduced to switching the overlay memories of SP for the external access from General-Purpose Processor (GP), which can be served as a System Controller (SC) based on a microcomputers (CPU, DSP and ICP). System Controllers should be based on DSP for control of local Interconnections in Crate, and special hardware (SCSI) or DSP with IDMA should be used for link to PC. Integrated Communication Processor (IPC) can be used as basic fragment for networking of Distributed Systems. Tasks loaded in GP and SP can be executed simultaneously. Advanced Architecture requires efficient high-speed interconnections between SC and PC or inside the multiprocessor Crates.

Some approaches to System Architecture are analyzed: tradition BUS-based and new NON-BUS Distributed Memory System Architectures:

1) *BUS-BASED Direct-Addressing System Architecture* with direct address access to distributed memory in DSP modules on the Bus in Crate. System uses fixed short Bus Links for connecting 2 - 8 DSP modules. This standard Architecture is used for modern compact multiprocessor systems including on DSP-based board.

2) *BUS-BASED Overlayed-Memory System Architecture* can be based on low-cost 16-bit DSP with overlayed memory on-chip. Data-flow transmission in Crates take less local processor time, because of using overlay memory in switching between GP (SC) and SP. This new Architectures can be efficiently used in high-speed multiprocessor systems on the base of 16-bit DSP with overlayed on-chip memory.

3) *NO-BUS Direct Addressing System Architecture* with point-to-point Interconnections and packet transfer protocol with split-transaction mode can be developed on the base of a new SCI standards or SCI-type simplified

protocols (RAMLINK, SYNCLINK) and high-speed DSP possible with Integrated CPU and ICP fragments.

The same fragmented microcomputer Core should be developed on the basic of new technology (single-chip DSP, CPU and ICP) for BUS as well as variants of NON-BUS (Ring-type) System Interconnection.

2 BUS-BASED RT-system architectures

Real-time Data Acquisition and Control Systems can be developed on the basis of existing modular equipment, completely new ones or mixed of new and old devices. The last approach is attractive, but requires a new compatible approach to System Architectures. One of the best ways to get a compatible extension is to use a new FASTCAMAC Recommendations.

Practicality of efficient and compatible modular system development is dictated by existing good equipment of previous generation systems in many laboratories, as well as requirements of the modern high-speed Data Acquisition Systems. Problems are reduced to development of new modular systems, compatible with existing modules (CAMAC), with pass-band extended up to values, comparable with modern standards (VME.VXI). FASTCAMAC system should includes 3 levels of compatible upgrades.

2.1 FASTCAMAC recommendations

The simplest modification of CAMAC protocol (primary standard for open-collector drivers) allows to enlarge a source send rate given in existing CAMAC sections 3 Mbytes by 2.5 times. For compatibility with the standard cycle stay unchangeable 400ns at the beginning and end of CAMAC cycle. A controller reads data on the front of the strobe S1. In this time functional module begins to transfer a following word. In the block transfer mode the process is repeated until full packed will be transfered. CAMAC Bus ensure transfers of impulses 200ns. Transfer of the S1-strobe sequence with the 200ns intervals will allow to enlarge a velocity up to 7.5 Mbytes/s. The rise time of Signals on the open-collector drivers is a limiting factor.

Using the three-states drivers (instead of open-collectors) allows to enlarge a data send rate up to 5 times (up to 15 Mbyte/s). In new FASTCAMAC modules and controllers, it is reasonable to use three-states drivers, which allow to get nearly alike both signal fronts transferred on bus. In this case, it is reasonable to use both fronts of the strobe S1 for the data transfer, that allows us to get a higher band of frequencies. Block transfer will be increased up to 15 Mbytes/s. Reduction of pulse duration and intervals (100HC) will ensure an increase to send rate up to 30 Mbytes/s. Further send rate increasing can be getting from the account of broad bus on 48 bits for data read /write (up to 60 Mbytes/s), however it is possible under the respective improvement of a bus links. Some existing boards can not satisfy all high-speed requirements.

The first manufacturing FASTCAMAC modules were designed by LeCroy:

- LeCroy CX040 - ADC for digitization of the form of the signal, four independent channels up to 500MC/s, built-in memory 32 Kb/channel, and impuls generator. Reading rate of information on CAMAC-bus up to 40 Mbytes/s.
- LeCroy CL510 - an universal module of the exchange by digital information, memory 512, 48-bit words, 59 differential ECL outputs, RS-485, is kept DSP TMS320C20 with the program in EPROM or with boot through CAMAC. Transfer speed on CAMAC-bus up to 60 MBytes/s.
- The first FASTCAMAC controller was marketed on the base of SCSI interface by Jorway.

2.2 BUS-BASED distributed memory systems and overlay

Single-chip DSP-based micromodular subsystems on the small board can be efficiently developed as a core fragments. Any module is constructed from this core fragments. One of the best core for system development is ADSP2181-based fragments. The Selected Distributed Memory System Architecture includes System Controller, based on a single-chip fix-point ADSP2181 - core fragment, which can be interfaced to PC with RS232 (slow systems), or IDMA (high-speed systems), or used with special Integrated Communication Processors (ICP). IDMA provides parallel channels for direct addressed transfers of data in both directions. ADSP2181 was selected as core element for Overlayed System Architecture. It's well agreed with requirements of signal processing, control tasks and protocols (FASTCAMAC) for low-cost system applications. ADSP2106x is selected as core fragment for high-end real-time systems.

ADSP2181 is one of the best cost-effective device for real-time Data Acquisition and Control systems. It uses fixed execution cycle (30 ns), IDMA, overlayed on-chip memory and flexible I/O. A shot constant cycle provides good real-time performance and can be used for different protocol applications and for signal processing. Each module can contain one or more DSP, one of which executes functions of the overlayed interaction with the SC and allows to use DSP as a built-in SP-fragment for real-time data-flow processing. Internal Direct Memory Access (IDMA) can be used for high-speed Interconnections in distributed systems.

The best device for network interconnections is communications ICP with ETHERNET supporting. It can be selected from the family of 16|32-bit ICP of Motorola:

– MC68302–16 bit RISC controller input-output, 16 MHz;
– MC68360–32 bit RISC controller, integrated with CPU32 + (QUICC);
– MPC860–32 bit RISC controller, integrated with 32 bit PowerPC;
– MC68356–16 bit RISC controller with 16/32-bit CPU and DSP 56002.

The optimal decision for 32-bit modular system communications now is MC68360, ensuring functions of the built-in microcomputer and ETHERNET network controller. New QUICC module consider as MC68302 development. It consists of 3 micromodules: CPU32+ (8.3 MIPS, 25 MHz), integrated with the memory controller

(supports SRAM, DRAM, EPROM) and communication RISC processor, maintaining communication protocols (ETHERNET, HDLC) for distributed networking systems. More priced MPC860 (PowerQUICC**)**, based on PowerPC kernel (53 MIPC, 40 MHz) includes 4K caches (commands and data), extended controller of the memory and Communication Processor (like MC68360). High-speed systems can be based on this ICP, but modern RT-Systems need in ICP with FASTETHERNET protocols.

Considered method of single-chip micromodular fragments for constructing of systems on the base of new technology (single-chip fixed- or floating-point DSP, CPU, ICP) allows to create a flexible DSP-based RT-Systems for Slow Control and high-speed Data Acquisition for experimental research on the same platform.

3 NON-BUS-BASED distributed memory systems

New NON-BUS Systems can be based on a new SCI or RT-SCI standards. SCI is high-priced Interconnections now. Other approaches for RT-systems can be based on simplified SCI-type protocols (like RAMLINK, SYNCLINK), which can be developed on the base of existing possibilities of new families of modern single-chip 16-bit ADSP2181 or 32-bit ADSP2106x fragments.

3.1 Simplified SCI-type protocol recommendations. (RAMLINK and SYNCLINK)

RAMLink uses point-to-point communication to achieve a simple high-bandwidth data-transfer path between a memory controller and one or more slaves devices. Having one controller on each ringlet simplifies the initialization and arbitration protocols. Each ringlet is limited to 62 slave addresses (62,83 are used for broadcast and idle-packet addresses). The basic links between nodes contain thirteen signals nine data signals, a clock reference signal, a strobe signal and a flag signal. The 9-th bit is provided to support 9-bit RAM. RAMLink changes data values on both edges of the clock. The hierarchical memory system has hybrid agent nodes, with at the levels of the hierarchy agent appear to be slave, but at the lower levels - to be controller. In the hierarchy topology different signaling may be utilized at different levels (at the higher levels - RAMLink, at the lower levels - SyncLink).

RAMLINK and SYNCLINK are two similar protocols, designed for a memory systems and extended I/O. Increased optimization for RAM applications and the reduced emphasis on I/O interfaces, a number of evolutionary changes have been made from the RamLink protocols to improve efficiency and take full advantage of the bus-like connections used by SyncLink. It adapts the RamLink to purely memory systems and specifies a packet-based interface for cost-effective communication between a memory controller and dynamic memory chips. This two approach has some differences:

- The SyncLink responses do not include any status information. In the rare cases, where status is needed, it must be saved within the SLDRAM chip for subsequent readout via special registers.
- The mechanism in RamLink, that allowed for responses to be returned earlier than the scheduled time has been eliminated.
- SyncLink scheduling is always exact, and there is no mechanism for the SLDRAM chip to request a retry (due to an unexpected conflict between refresh and access).
- Response packets only occur when scheduled, so need not identify themselves to the controller. Bandwidth is saved by eliminating the header and the status information. Thus responses occur for reads (contain data only).
- To make the scheduling fully predictable, it's recommended to eliminate the need for retry, and simplify the SyncLink design. Self-refresh is not supported during normal operation, though it is expected to be used while in low-power standby modes.
- To improve efficiency, the request-packet headers have been reduced to the minimum necessary for SLDRAM applications
- SyncLink RAMs are not expected to have internal request or response queues, but merely to handle one request and one response per block. Multiple blocks have the same read/write timing as independent SLDRAM.

SyncLink is intended to be an interconnect standard that suited to memory arrays. The primary goal of SyncLink is to support low-cost commodity SLDRAM parts. The following objectives were assumed or developed during the development of this standard :

- The SyncLink interface should be applicable to a majority of future DRAM applications.
- The SyncLink interface should allow memory controllers to schedule the responses for multiple concurrently active requests.
- The SyncLink interface should support other RAM-like components, if they emulate the characteristics of RAM-chip components, including ROM and FLASH memories; High-bandwidth I/O devices; Bridges to other Interconnect (such as SCI).

The support of other devices should be consistent with this goal; thus device and bridge interfaces should be sufficient but may be suboptimal. The design strategy was SLDRAM simplicity and Interoperable speeds. Mixed-speed DRAM components can be supported by a simple controller that assumes the slowest DRAM access time for all. The scope of the SyncLink definition is given below:

1) The SyncLink interface uses RamLink-like protocols to communicate between a controller and one or more memory devices.
2) The SyncLink interface specifies signals used to communicate between the controller and one or more SLDRAMs. Other standards are referenced for detailed signal levels and timing characteristics.
3) The SyncLink interface does not specify physical packaging requirements. Other standards groups (JEDEC) are expected to define physical-packaging standards based on market requirements.

3.2 NON-BUS-BASED distributed memory systems

The new proposed approach to System development is based on two-level hierarchical Model:

1) Interconnection for Modular Systems in the Crate, which has fixed length Ring-like two-bus Links and can be used for up to 16-32 DSP in RT-Systems (GP as a Master module and SP) - as slaves. It is good idea to use in this systems the same overlayed memory approach.

2) RING Interconnection between number of SC and PC with point-to-point links (different distance) for distributed systems. A single Master SC on the base of 32-bit DSP partitions his address field to target Slave SC (RTSystem nodes) and can addressed them by sending request packet. The addressed node (Slave SC) send the response packet to the Master SC. Up to 4 transactions can be performed at the same time in one RINGLet.

RT-Systems for Data Acquisition and Control Applications can be based on RAMLink-type protocols with single Master SC and many Slaves DSP-nodes connected in small RINGLets. Fixed length FASTCAMAC Crates can be used for two-bus RING-type Interconnections with protocol simulated on the base of ADSP2181 algorithms as the first step (possible in the same FASTCAMAC).

Making the module systems with the portioned memory requires presence large powered 32-bit DSP, for which effectively can be used ADSP2106x. It has 2 Mbytes memory in crystal, extended input-output and IDMA. It can be used as Master SC in the PC board or built fragment in target system. It can be connected to distributed target SC in Crates on the base of RS232 (slow systems) or with IDMA and in high-speed networks and advanced Interconnections .

Resume

1. Summary of Recommendation for FAST-CAMAC compatible Extension

1 level *(L1)* - defines a possibility of the data-flow transfer on 24-bits bus in the block mode on strobes S1 length and gap 200ns by means of open-collector circuits that ensures a transfer rate up to 7.5 Mbytes/with. Data are received on the single front of S1 strobe. The next word of the block is transferred on the bus at the S1 rise front. Distance between fronts of nearby strobes ~400 ns. Strobe S2 is formed in the last FASTCAMAC cycle for compatibility with the basic standard protocol.

2 levels *(L2)* - defines an using the 3-states drivers (circuits with open-collector are not excluded). L2 allows a data transfer on both strobes fronts and ensures a possibility of the S1 pulse length reduction and gaps between them. Entering the 3-states drivers is reasonable for new system developments (up to 15 Mbytes/s). Strobe and interval duration can be shortened to 100 ns (up to 30 Mbytes/s).

3 levels *(L3)* defines an extension of the bus for the data communications (48 bits) and allows to bring a send rate of the block up to 60 Mbytes/s. L3 uses all lines (R1-24 and W1-24) as both direction 48-bit bus.

2. Functions of the System Controller for data acquisition and realization of interaction protocols in the modules, as well as quick processing the signals and other tasks of the real-time applications can based effectively on the modern high-speed DSP, complemented by meanses of communication with other parts of the system and Personal Computer by the networking. One of the best way is using ICP with Ethernet protocol and for future fast systems ICP should be with FASTETHERNET protocol.

3. The basic single-chip microcomputer for modular systems as low-price core fragment for RT-Systems can be select ADSP2181, which can be used efficiently for compatible extension FASTCAMAC, as well as developments of new more efficient modular systems with overlayed memory. For high-end RT-Systems with Distributed Memory Architecture should be used 32-bit ADSP2106x on System Controller (and module) level.

4. Advanced low-cost RT-System can be based on simplified SCI-type RAMLINK-like protocol for hierarchical structures in Data Acquisition and Control applications.

References

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[4] IEEE1596.4. RAMLink standard.

[5] IEEE P1596.7-199X. SyncLink Draft.

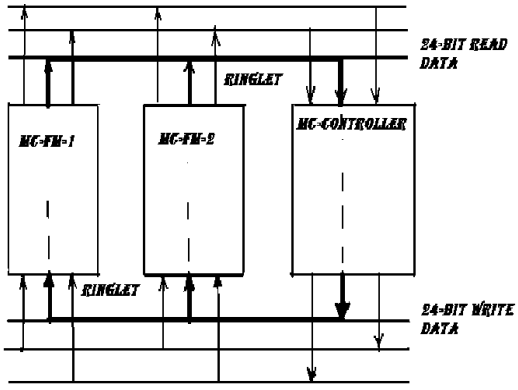

Fig. 1 Ring type modular structure in CAMAC crate.

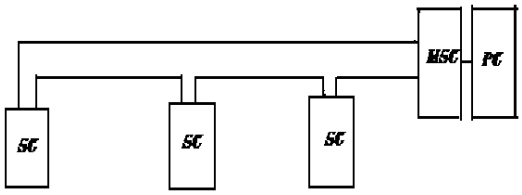

Fig. 2 Ringlet with master system controller (MSDC) connected to up 62 slave SC